SONY

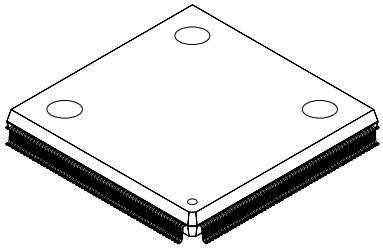
CXD2467AQ

Digital Signal Driver/Timing Generator

Description

The CXD2467AQ incorporates digital signal processor type RGB driver and timing generator functions onto a single IC. Operation is possible with a system clock up to 135MHz (max.). This IC can process video signals in bands up to SXGA standard, and can output the timing signals for driving various LCD panels such as SXGA (LCX028) and XGA (LCX017 and LCX023).

240 pin QFP (Plastic)



Features

- Various picture quality adjustment functions such as user adjustment, white balance adjustment and gamma correction
- OSD MIX, black frame processing, mute and limiter functions
- Drives various data projector LCD panels such as SXGA (LCX028) and XGA (LCX017 and LCX023)
- Controls the sample-and-hold position of the CXA2112R sample-and-hold driver
- Line inversion and field inversion signal generation
- Supports AC drive of LCD panels during no signal

Absolute Maximum Ratings (V_{SS} = 0V)

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +4.0	V
• Input voltage	V_I	Vss – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	Vss – 0.5 to V_{DD} + 0.5	V
• Storage temperature	Tstg	–55 to +125	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	3.0 to 3.6	V
• Operating temperature	Topr	–20 to +75	°C

Applications

LCD projectors and other video equipment

Structure

Silicon gate CMOS IC

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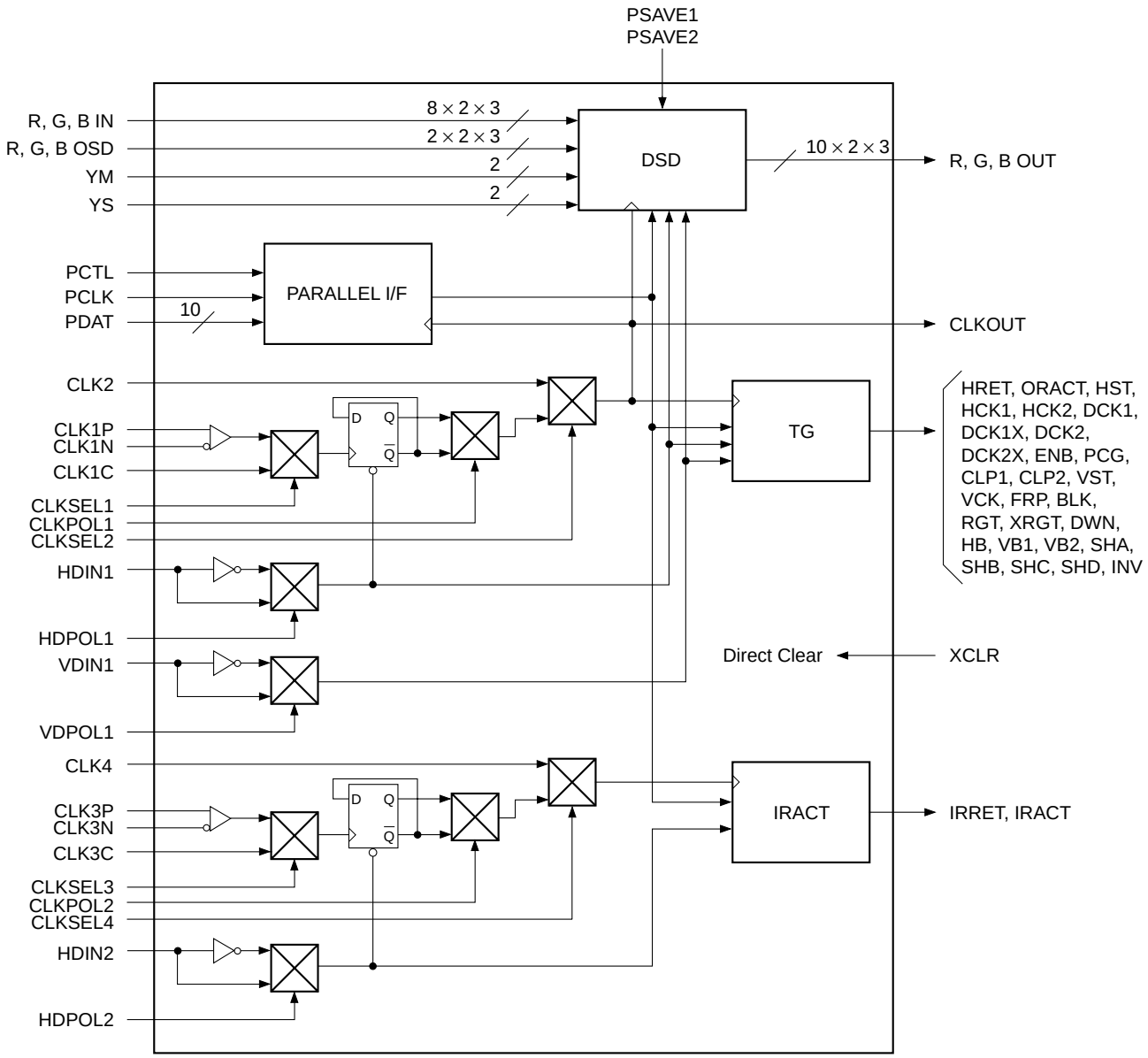
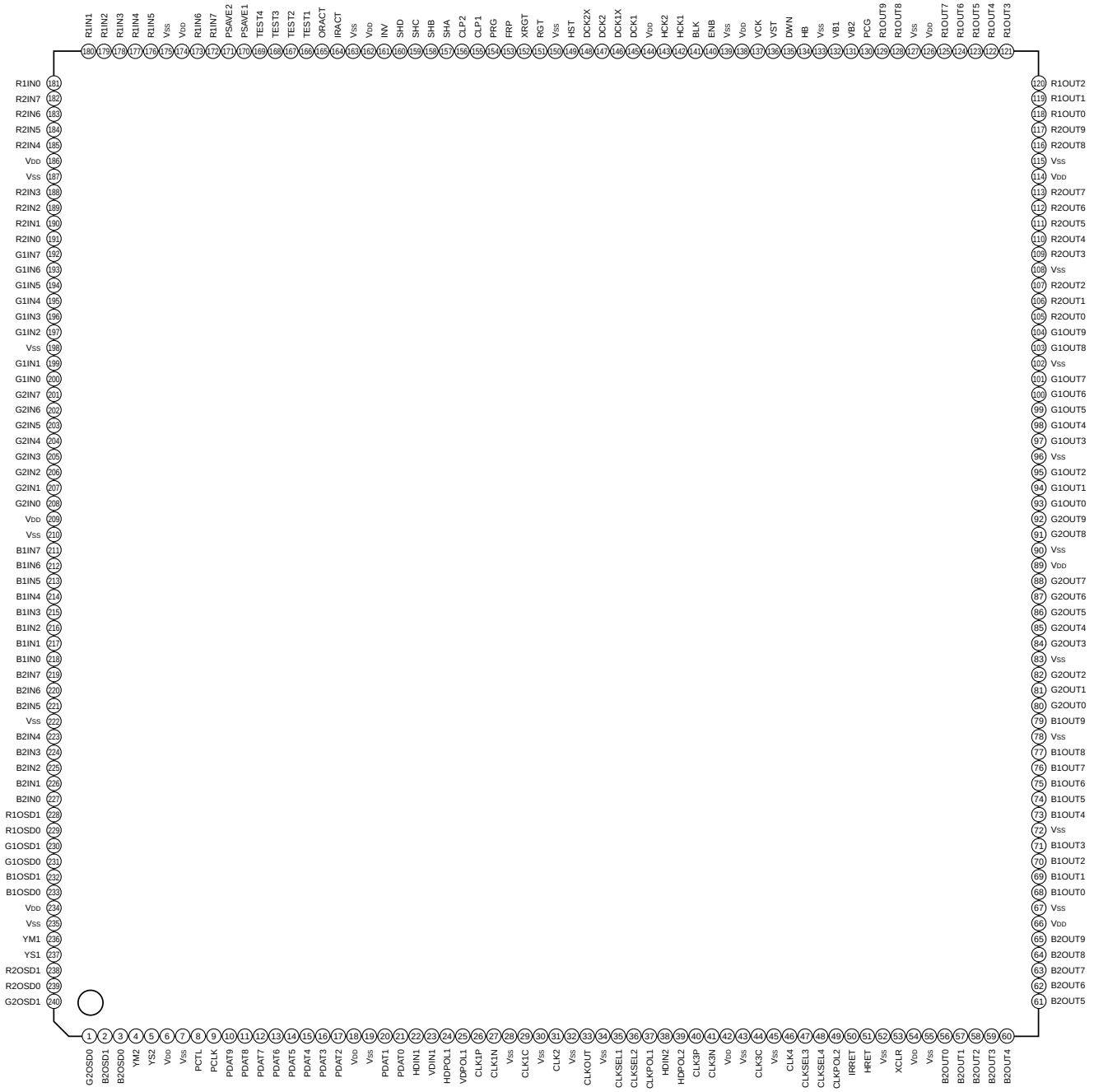
E99613A08

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description	Input pin processing for open status
1	G2OSD0	I	OSD green data input (port 2)	—
2	B2OSD1	I	OSD blue data input (port 2)	—
3	B2OSD0	I	OSD blue data input (port 2)	—
4	YM2	I	OSD YM input (port 2)	L
5	YS2	I	OSD YS input (port 2)	L
6	V_{DD}	—	Power supply	—
7	V_{SS}	—	GND	—
8	PCTL	I	Parallel I/F control signal input	H
9	PCLK	I	Parallel I/F clock input	—
10	PDAT9	I	Parallel I/F data input	—
11	PDAT8	I	Parallel I/F data input	—
12	PDAT7	I	Parallel I/F data input	—
13	PDAT6	I	Parallel I/F data input	—
14	PDAT5	I	Parallel I/F data input	—
15	PDAT4	I	Parallel I/F data input	—
16	PDAT3	I	Parallel I/F data input	—
17	PDAT2	I	Parallel I/F data input	—
18	V_{DD}	—	Power supply	—
19	V_{SS}	—	GND	—
20	PDAT1	I	Parallel I/F data input	—
21	PDAT0	I	Parallel I/F data input	—
22	HDIN1	I	Horizontal sync signal input-1	—
23	VDIN1	I	Vertical sync signal input-1	—
24	HDPOL1	I	HDIN1 input polarity selection (High: positive polarity, Low: negative polarity)	L
25	VDPOL1	I	VDIN1 input polarity selection (High: positive polarity, Low: negative polarity)	L
26	CLK1P	I	Clock input-1 (small-amplitude differential input, positive polarity)	—
27	CLK1N	I	Clock input-1 (small-amplitude differential input, negative polarity)	—
28	V_{SS}	—	GND	—
29	CLK1C	I	Clock input-1 (CMOS input)	—
30	V_{SS}	—	GND	—
31	CLK2	I	1/2 frequency-divided clock input-1 (CMOS input)	—
32	V_{SS}	—	GND	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
33	CLKOUT	O	1/2 frequency-divided clock output	—
34	Vss	—	GND	—
35	CLKSEL1	I	Input clock selection (High: CLK1C, Low: CLK1P, N)	L
36	CLKSEL2	I	Input clock selection (High: CLK2, Low: CLK1)	L
37	CLKPOL1	I	1/2 frequency division circuit output selection (High: XQ output, Low: Q output)	L
38	HDIN2	I	Horizontal sync signal input-2	—
39	HDPOL2	I	HDIN2 input polarity selection (High: positive polarity, Low: negative polarity)	L
40	CLK3P	I	Clock input-2 (small-amplitude differential input, positive polarity)	—
41	CLK3N	I	Clock input-2 (small-amplitude differential input, negative polarity)	—
42	V_{DD}	—	Power supply	—
43	V_{SS}	—	GND	—
44	CLK3C	I	Clock input-2 (CMOS input)	—
45	V_{SS}	—	GND	—
46	CLK4	I	1/2 frequency-divided clock input-2 (CMOS input)	—
47	CLKSEL3	I	Input clock selection (High: CLK3C, Low: CLK3P, N)	L
48	CLKSEL4	I	Input clock selection (High: CLK4, Low: CLK3)	L
49	CLKPOL2	I	1/2 frequency division circuit output selection (High: XQ output, Low: Q output)	L
50	IRRET	O	Auxiliary pulse output	—
51	HRET	O	Auxiliary pulse output	—
52	V_{SS}	—	GND	—
53	XCLR	I	External clear (Low: reset)	H
54	V_{DD}	—	Power supply	—
55	V_{SS}	—	GND	—
56	B2OUT0	O	Blue data output (port 2)	—
57	B2OUT1	O	Blue data output (port 2)	—
58	B2OUT2	O	Blue data output (port 2)	—
59	B2OUT3	O	Blue data output (port 2)	—
60	B2OUT4	O	Blue data output (port 2)	—
61	B2OUT5	O	Blue data output (port 2)	—
62	B2OUT6	O	Blue data output (port 2)	—
63	B2OUT7	O	Blue data output (port 2)	—
64	B2OUT8	O	Blue data output (port 2)	—
65	B2OUT9	O	Blue data output (port 2)	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
66	V_{DD}	—	Power supply	—
67	Vss	—	GND	—
68	B1OUT0	O	Blue data output (port 1)	—
69	B1OUT1	O	Blue data output (port 1)	—
70	B1OUT2	O	Blue data output (port 1)	—
71	B1OUT3	O	Blue data output (port 1)	—
72	V_{SS}	—	GND	—
73	B1OUT4	O	Blue data output (port 1)	—
74	B1OUT5	O	Blue data output (port 1)	—
75	B1OUT6	O	Blue data output (port 1)	—
76	B1OUT7	O	Blue data output (port 1)	—
77	B1OUT8	O	Blue data output (port 1)	—
78	V_{SS}	—	GND	—
79	B1OUT9	O	Blue data output (port 1)	—
80	G2OUT0	O	Green data output (port 2)	—
81	G2OUT1	O	Green data output (port 2)	—
82	G2OUT2	O	Green data output (port 2)	—
83	V_{SS}	—	GND	—
84	G2OUT3	O	Green data output (port 2)	—
85	G2OUT4	O	Green data output (port 2)	—
86	G2OUT5	O	Green data output (port 2)	—
87	G2OUT6	O	Green data output (port 2)	—
88	G2OUT7	O	Green data output (port 2)	—
89	V_{DD}	—	Power supply	—
90	V_{SS}	—	GND	—
91	G2OUT8	O	Green data output (port 2)	—
92	G2OUT9	O	Green data output (port 2)	—
93	G1OUT0	O	Green data output (port 1)	—
94	G1OUT1	O	Green data output (port 1)	—
95	G1OUT2	O	Green data output (port 1)	—
96	V_{SS}	—	GND	—
97	G1OUT3	O	Green data output (port 1)	—
98	G1OUT4	O	Green data output (port 1)	—
99	G1OUT5	O	Green data output (port 1)	—
100	G1OUT6	O	Green data output (port 1)	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
101	G1OUT7	O	Green data output (port 1)	—
102	V_{SS}	—	GND	—
103	G1OUT8	O	Green data output (port 1)	—
104	G1OUT9	O	Green data output (port 1)	—
105	R2OUT0	O	Red data output (port 2)	—
106	R2OUT1	O	Red data output (port 2)	—
107	R2OUT2	O	Red data output (port 2)	—
108	V_{SS}	—	GND	—
109	R2OUT3	O	Red data output (port 2)	—
110	R2OUT4	O	Red data output (port 2)	—
111	R2OUT5	O	Red data output (port 2)	—
112	R2OUT6	O	Red data output (port 2)	—
113	R2OUT7	O	Red data output (port 2)	—
114	V_{DD}	—	Power supply	—
115	V_{SS}	—	GND	—
116	R2OUT8	O	Red data output (port 2)	—
117	R2OUT9	O	Red data output (port 2)	—
118	R1OUT0	O	Red data output (port 1)	—
119	R1OUT1	O	Red data output (port 1)	—
120	R1OUT2	O	Red data output (port 1)	—
121	R1OUT3	O	Red data output (port 1)	—
122	R1OUT4	O	Red data output (port 1)	—
123	R1OUT5	O	Red data output (port 1)	—
124	R1OUT6	O	Red data output (port 1)	—
125	R1OUT7	O	Red data output (port 1)	—
126	V_{DD}	—	Power supply	—
127	V_{SS}	—	GND	—
128	R1OUT8	O	Red data output (port 1)	—
129	R1OUT9	O	Red data output (port 1)	—
130	PCG	O	PCG pulse output	—
131	VB2	O	VB2 signal output	—
132	VB1	O	VB1 signal output	—
133	V_{SS}	—	GND	—
134	HB	O	HB signal output	—
135	DWN	O	Up/down inversion signal output	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
136	VST	O	V start pulse output	—
137	VCK	O	V clock pulse output	—
138	V_{DD}	—	Power supply	—
139	V_{SS}	—	GND	—
140	ENB	O	ENB pulse output	—
141	BLK	O	BLK pulse output	—
142	HCK1	O	H clock pulse output 1	—
143	HCK2	O	H clock pulse output 2 (reversed phase)	—
144	V_{DD}	—	Power supply	—
145	DCK1	O	Auxiliary pulse output	—
146	DCK1X	O	Auxiliary pulse output	—
147	DCK2	O	Auxiliary pulse output	—
148	DCK2X	O	Auxiliary pulse output	—
149	HST	O	H start pulse output	—
150	V_{SS}	—	GND	—
151	RGT	O	Left/right inversion signal output	—
152	XRGT	O	Left/right inversion signal output (reversed polarity)	—
153	FRP	O	AC drive inversion pulse output	—
154	PRG	O	PRG pulse output	—
155	CLP1	O	Pedestal clamp pulse output 1	—
156	CLP2	O	Pedestal clamp pulse output 2	—
157	SHA	O	External sample-and-hold driver control signal output	—
158	SHB	O	External sample-and-hold driver control signal output	—
159	SHC	O	External sample-and-hold driver control signal output	—
160	SHD	O	External sample-and-hold driver control signal output	—
161	INV	O	External sample-and-hold driver control signal output	—
162	V_{DD}	—	Power supply	—
163	V_{SS}	—	GND	—
164	IRACT	O	Auxiliary pulse output	—
165	ORACT	O	Auxiliary pulse output	—
166	TEST1	—	Test pin (Connect to GND.)	—
167	TEST2	—	Test pin (Connect to GND.)	—
168	TEST3	—	Test pin (Connect to V_{DD}.)	—
169	TEST4	—	Test pin (Connect to V_{DD}.)	—
170	PSAVE1	I	Power saving pin (High: standby status, Low: normal status)	L

Pin No.	Symbol	I/O	Description	Input pin processing for open status
171	PSAVE2	I	Power saving pin (High: standby status, Low: normal status)	L
172	R1IN7	I	Red data input (port 1)	—
173	R1IN6	I	Red data input (port 1)	—
174	V_{DD}	—	Power supply	—
175	V_{SS}	—	GND	—
176	R1IN5	I	Red data input (port 1)	—
177	R1IN4	I	Red data input (port 1)	—
178	R1IN3	I	Red data input (port 1)	—
179	R1IN2	I	Red data input (port 1)	—
180	R1IN1	I	Red data input (port 1)	—
181	R1IN0	I	Red data input (port 1)	—
182	R2IN7	I	Red data input (port 2)	—
183	R2IN6	I	Red data input (port 2)	—
184	R2IN5	I	Red data input (port 2)	—
185	R2IN4	I	Red data input (port 2)	—
186	V_{DD}	—	Power supply	—
187	V_{SS}	—	GND	—
188	R2IN3	I	Red data input (port 2)	—
189	R2IN2	I	Red data input (port 2)	—
190	R2IN1	I	Red data input (port 2)	—
191	R2IN0	I	Red data input (port 2)	—
192	G1IN7	I	Green data input (port 1)	—
193	G1IN6	I	Green data input (port 1)	—
194	G1IN5	I	Green data input (port 1)	—
195	G1IN4	I	Green data input (port 1)	—
196	G1IN3	I	Green data input (port 1)	—
197	G1IN2	I	Green data input (port 1)	—
198	V_{SS}	—	GND	—
199	G1IN1	I	Green data input (port 1)	—
200	G1IN0	I	Green data input (port 1)	—
201	G2IN7	I	Green data input (port 2)	—
202	G2IN6	I	Green data input (port 2)	—
203	G2IN5	I	Green data input (port 2)	—
204	G2IN4	I	Green data input (port 2)	—
205	G2IN3	I	Green data input (port 2)	—

Pin No.	Symbol	I/O	Description	Input pin processing for open status
206	G2IN2	I	Green data input (port 2)	—
207	G2IN1	I	Green data input (port 2)	—
208	G2IN0	I	Green data input (port 2)	—
209	V_{DD}	—	Power supply	—
210	V_{SS}	—	GND	—
211	B1IN7	I	Blue data input (port 1)	—
212	B1IN6	I	Blue data input (port 1)	—
213	B1IN5	I	Blue data input (port 1)	—
214	B1IN4	I	Blue data input (port 1)	—
215	B1IN3	I	Blue data input (port 1)	—
216	B1IN2	I	Blue data input (port 1)	—
217	B1IN1	I	Blue data input (port 1)	—
218	B1IN0	I	Blue data input (port 1)	—
219	B2IN7	I	Blue data input (port 2)	—
220	B2IN6	I	Blue data input (port 2)	—
221	B2IN5	I	Blue data input (port 2)	—
222	V_{SS}	—	GND	—
223	B2IN4	I	Blue data input (port 2)	—
224	B2IN3	I	Blue data input (port 2)	—
225	B2IN2	I	Blue data input (port 2)	—
226	B2IN1	I	Blue data input (port 2)	—
227	B2IN0	I	Blue data input (port 2)	—
228	R1OSD1	I	OSD red data input (port 1)	—
229	R1OSD0	I	OSD red data input (port 1)	—
230	G1OSD1	I	OSD green data input (port 1)	—
231	G1OSD0	I	OSD green data input (port 1)	—
232	B1OSD1	I	OSD blue data input (port 1)	—
233	B1OSD0	I	OSD blue data input (port 1)	—
234	V_{DD}	—	Power supply	—
235	V_{SS}	—	GND	—
236	YM1	I	OSD YM input (port 1)	L
237	YS1	I	OSD YS input (port 1)	L
238	R2OSD1	I	OSD red data input (port 2)	—
239	R2OSD0	I	OSD red data input (port 2)	—
240	G2OSD1	I	OSD green data input (port 2)	—

* H: Pull-up, L: Pull-down

Electrical Characteristics

DC Characteristics

(V_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Applicable pins	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	—	—	3.0	3.3	3.6	V
Input voltage 1	V_{IH1}	CLK1C, CLK2 CLK3C, CLK4	CMOS input cell	0.65V_{DD}	—	V_{DD} + 0.3	
	V_{IL1}			V_{SS}	—	0.25V_{DD}	
Input voltage 2	V_{IH2}	*1	CMOS Schmitt trigger input cell	0.8V_{DD}	—	V_{DD} + 0.3	
	V_{IL2}			V_{SS}	—	0.2V_{DD}	
Input voltage 3	VC (center level)	CLK1P, CLK1N CLK3P, CLK3N	Small-amplitude differential input	(V_{DD} × 0.606) – 0.1	V_{DD} × 0.606	(V_{DD} × 0.606) + 0.1	
	V_{IH3}*2			V_{IL3} + 0.3	—	V_{DD}	
	V_{IL3}*2			V_{SS}	—	V_{IH3} – 0.3	
Output voltage	V_{OH}	All output pins	—	V_{DD} – 0.5	—	V_{DD}	
	V_{OL}		—	V_{SS}	—	0.4	
Current consumption	I_{DD}	—	CLK = 135MHz V_{DD} = 3.3V Output load = 30pF	—	—	490	mA
			*3			360	

*1 Input pins other than those indicated in items Input voltage 1 and Input voltage 3.
*2 V_{IH3} > (Maximum VC value) and V_{IL3} < (Minimum VC value).
*3 PSAVE1 = PSAVE2 = H

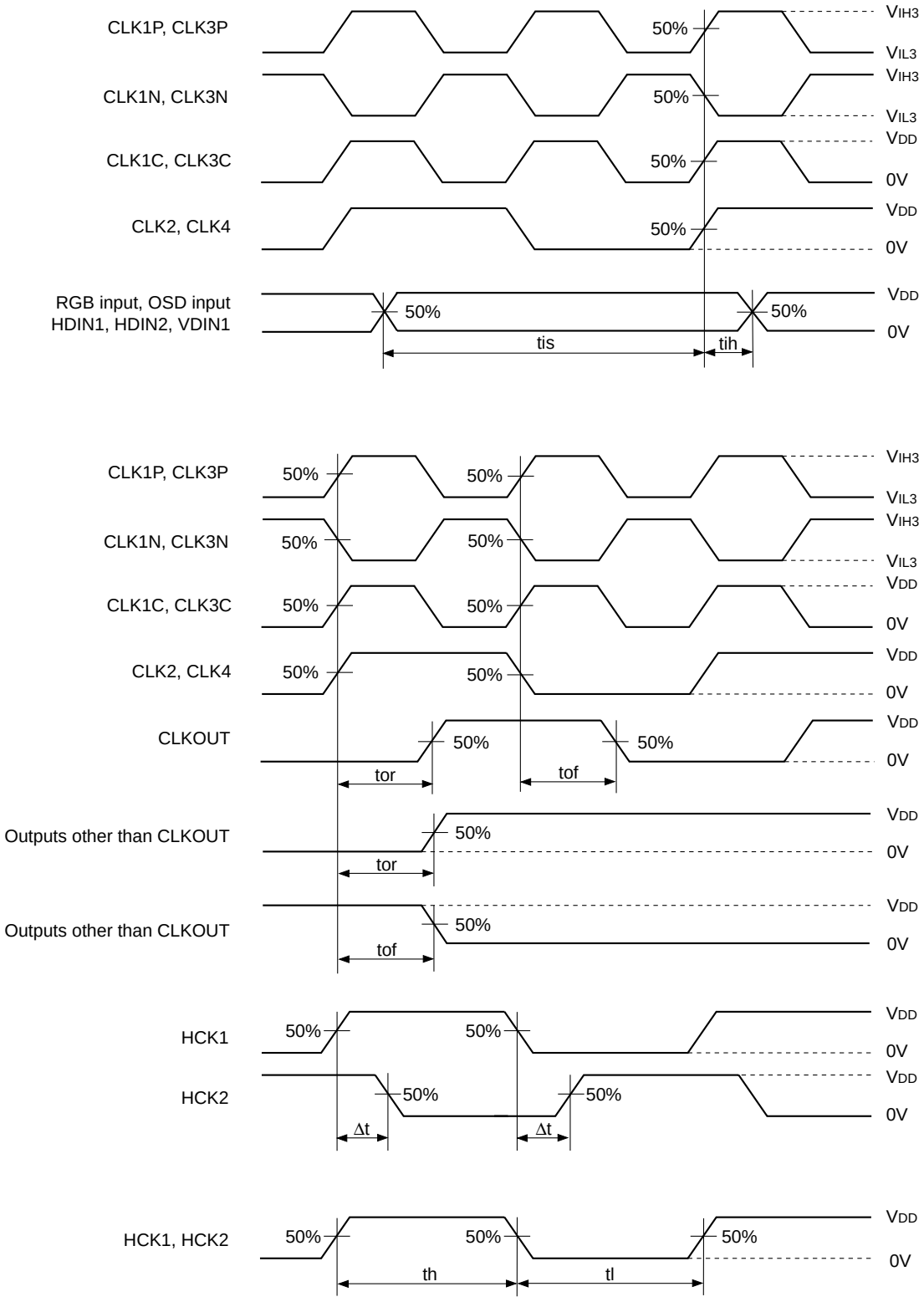
AC Characteristics

(V_{DD} = 3.3 ± 0.3V, V_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Applicable pins	Conditions	Min.	Typ.	Max.	Unit
Clock input cycle	—	CLK1, CLK3	—	7.4	—	—	ns
		CLK2, CLK4	—	14.8	—	—	
Input setup time	tis	*4	—	3.5	—	—	
Input hold time	tih	*4	—	1.5	—	—	
Output rise/fall delay time	tor/tof	HCK1, HCK2, HST	CL = 90pF	9	12	19	
Output rise/fall delay time	tor/tof	PCG, VST, VCK, ENB, BLK	CL = 50pF	9	12	19	
Output rise/fall delay time	tor/tof	CLKOUT	CL = 50pF	8	11	18	
Output rise/fall delay time	tor/tof	All other output pins	CL = 30pF	9	12	19	
Cross-point time difference	Δt	HCK1, HCK2	CL = 90pF	–5	—	5	
Cross-point time difference	Δt	HCK1, HCK2	CL = 90pF	48	50	52	

*4 RGB input, OSD input, HDIN1, HDIN2, VDIN

Timing Definition

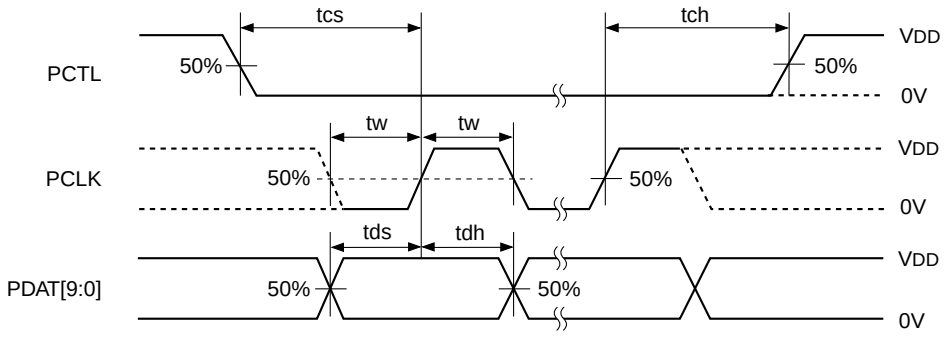


Parallel Transfer Data AC Characteristics (V_{DD} = 3.3 ± 0.3V, V_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Min.	Typ.	Max.
PCTL setup time with respect to rise of PCLK	tcs	8T*5	—	—
PCTL hold time with respect to rise of PCLK	tch	8T	—	—
PDAT[9:0] setup time with respect to rise of PCLK	tds	4T	—	—
PDAT[9:0] hold time with respect to rise of PCLK	tdh	4T	—	—
PCLK pulse width	tw	4T	—	—

*5 T: Master clock (CLK1P/CLK1N, CLK1C, CLK3P/CLK3N, CLK3C) cycle [ns]

Timing Definition



Description of Operation

1. DSD and TG Blocks

1-1. Description of Input/Output Pins

(a) Sync signal input pins (HDIN1 and VDIN1)

Horizontal and vertical separate sync signals are input to HDIN1 (Pin 22) and VDIN1 (Pin 23), respectively. The CXD2467AQ supports only non-interlace sync signals with a dot clock of 135MHz or less. Also, the HSYNC width should be 40 dot clocks or more, and the VSYNC width, 1H or more.

(b) Sync signal polarity setting pins (HDPOL1 and VDPOL1)

The polarity of the input horizontal and vertical sync signals are set by HDPOL1 (Pin 24) and VDPOL1 (Pin 25), respectively. Set to high level for positive polarity, and to low level for negative polarity.

(c) Master clock input pins (CLK1P/CLK1N, CLK1C and CLK2) and clock selection pins (CLKSEL1 and CLKSEL2)

Phase comparison is performed by an external circuit and a clock synchronized to the sync signal is input. The 1/N (N is the number of clocks during one horizontal period) frequency-divided dot clock pulse is output from HRET (Pin 51) for the external phase comparator.

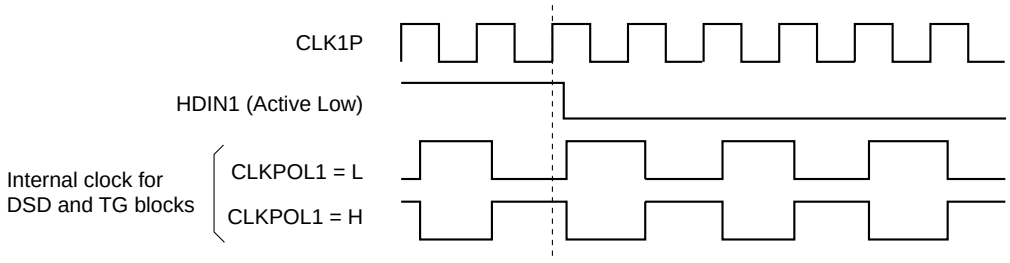
The master clock input pins consist of CLK1P/CLK1N (Pins 26 and 27) for small-amplitude differential input (center level: 2.0V, amplitude: ±0.4V), and CLK1C (Pin 29) and CLK2 (Pin 31) for CMOS level input for a total of three channels. These are selected according to CLKSEL1 (Pin 35) and CLKSEL2 (Pin 36).

CLKSEL1	CLKSEL2	Selected clock input pins
L	L	CLK1P/CLK1N (small-amplitude differential input, input at the same frequency as the dot clock)
H	L	CLK1C (CMOS level input, input at the same frequency as the dot clock)
—	H	CLK2 (CMOS level input, input at 1/2 the frequency of the dot clock)

—: Don't care

(d) Clock polarity switching pin (CLKPOL1)

When CLK1P/1N or CLK1C is selected, the clock is 1/2 frequency divided inside the IC using the falling edge of the HD pulse as the reference. The polarity of this 1/2 frequency-divided clock is switched by CLKPOL1 (Pin 37). Normally CLKPOL1 is used at low level.



(e) RGB signal input pins (R1IN, R2IN, G1IN, G2IN, B1IN and B2IN)

These pins input RGB signals that have been demultiplexed to 1:2. The Red signal is input to R1IN (Pins 172, 173 and 176 to 181) and R2IN (Pins 182 to 185 and 188 to 191), the Green signal to G1IN (Pins 192 to 197, 199 and 200) and G2IN (Pins 201 to 208), and the Blue signal to B1IN (Pins 211 to 218) and B2IN (Pins 219 to 221 and 223 to 227).

(f) OSD signal input pins (R1OSD, R2OSD, G1OSD, G2OSD, B1OSD, B2OSD, YM1, YM2, YS1 and YS2)

These pins input OSD signals that have been demultiplexed to 1:2. The Red signal is input to R1OSD (Pins 228 and 229) and R2OSD (Pins 238 and 239), the Green signal to G1OSD (Pins 230 and 231) and G2OSD (Pins 1 and 240), and the Blue signal to B1OSD (Pins 232 and 233) and B2OSD (Pins 2 and 3). In addition, the YM signal is input to YM1 (Pin 236) and YM2 (Pin 4), and the YS signal to YS1 (Pin 237) and YS2 (Pin 5).

(g) Clock output pin (CLKOUT)

The internal master clock is output from CLKOUT (Pin 33).

(h) RGB signal output pins (R1OUT, R2OUT, G1OUT, G2OUT, B1OUT and B2OUT)

These pins output the arithmetically processed RGB signals in the 1:2 demultiplexed state. The Red signal is output from R1OUT (Pins 118 to 125, 128 and 129) and R2OUT (Pins 105 to 107, 109 to 113, 116 and 117), the Green signal from G1OUT (Pins 93 to 95, 97 to 101, 103 and 104) and G2OUT (Pins 80 to 82, 84 to 88, 91 and 92), and the Blue signal from B1OUT (Pins 68 to 71, 73 to 77 and 79) and B2OUT (Pins 56 to 65).

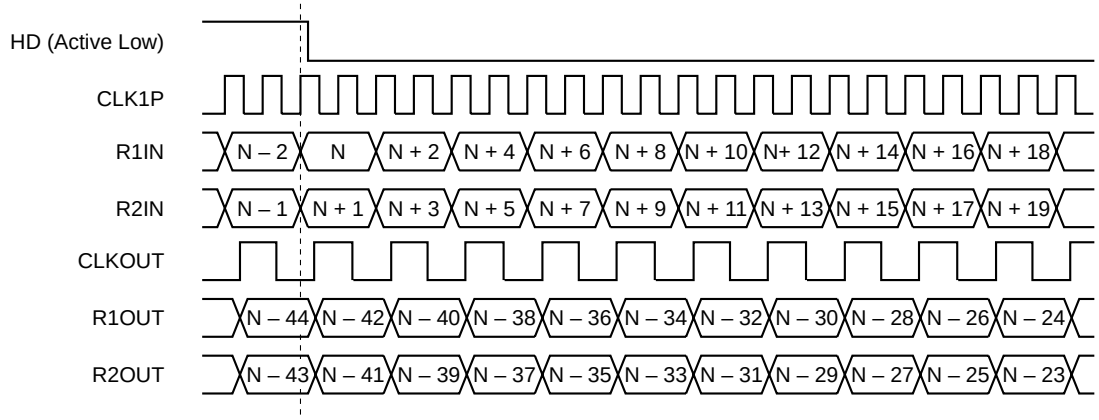
(i) Power saving pins (PSAVE1 and PSAVE2)

The gamma block RAM can be set to standby mode using both PSAVE1 (Pin 170) and PSAVE2 (Pin 171). The RAM operates normally when these pins are set to low level, and enters standby mode to reduce power consumption when set to high level. At this time data can not be set to or read from the RAM. However, data set in advance in the RAM is held even in standby mode. In addition, the gamma block RAM output is the data held just before the pin voltage changes to high level, so the RAM output changes according to the data set in the RAM, etc. Therefore, using the mute function to fix the CXD2467AQ output to the desired level in standby mode is recommended.

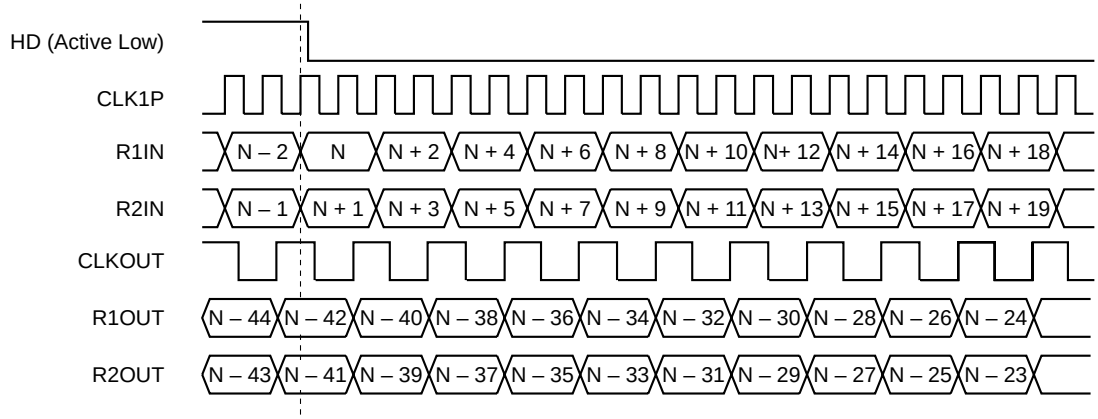
1-2. RGB Signal and OSD Signal Pipeline Delay

The RGB signal I/O pipeline delay is 42 dot clocks. In addition, the OSD, YM and YS signal pipeline delay is 12 dot clocks. Note that the phase relationship between each clock and the RGB signals is as shown in the figures below. This relationship is the same for the OSD, YM and YS signals.

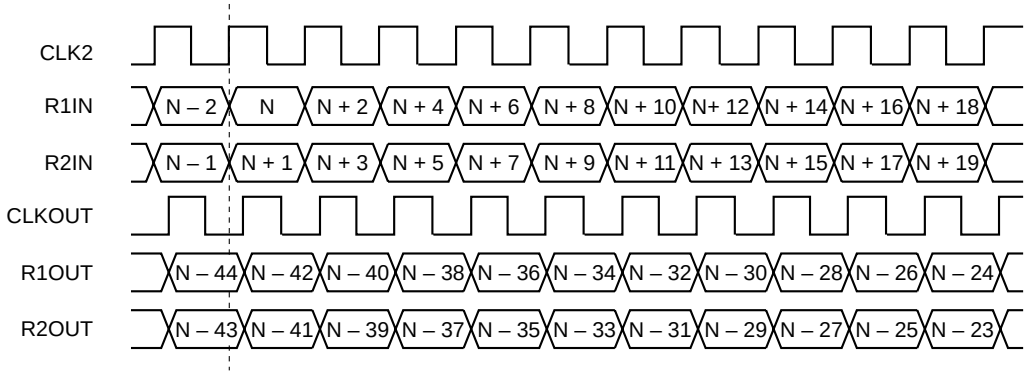
(1) CLK1P/CLK1N and CLK1C input (CLKPOL1 = low)



(2) CLK1P/CLK1N and CLK1C input (CLKPOL1 = high)

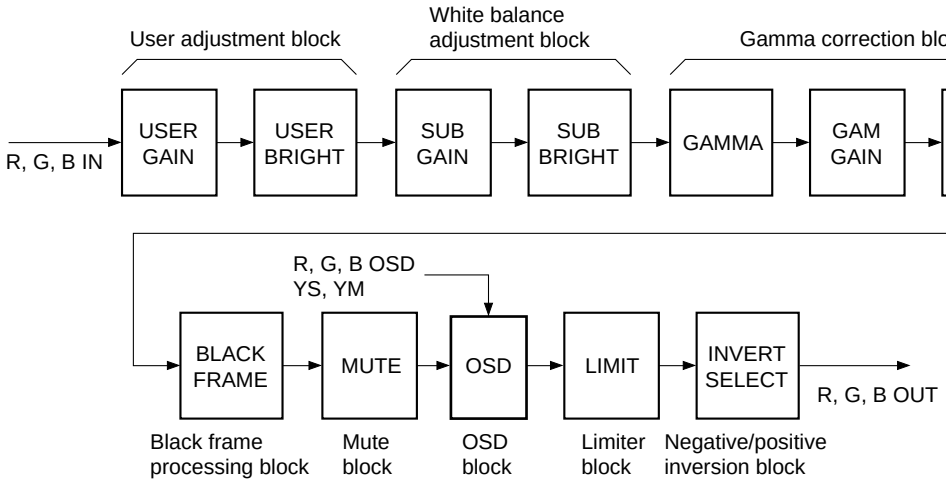


(3) CLK2 input



1-3. Description of DSD Block Signal Processing Functions

The DSD block signal processing flow is shown below. The input RGB signals undergo fine picture quality adjustment in the order of user adjustment, white balance adjustment and gamma correction. Further, the CXD2467AQ is also equipped with various adjustment functions such as black frame processing, mute, OSD, limiter, and negative/positive inversion.



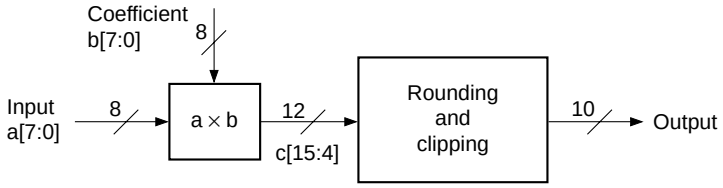
The various signal processing functions are described below. Note that the coefficients used for each arithmetic operation are set through the parallel I/F block. See the individual descriptions of each parallel I/F block item for a detailed description of the parallel I/F block.

(a) User gain block

This block performs multiplication processing as the user gain adjustment. Multiplication is performed as follows using the 8-bit data a[7:0] input to this IC and an 8-bit coefficient b[7:0].

$$c[15:0] = a[7:0] \times b[7:0]$$

The upper 12 bits c[15:4] of the arithmetic results are output. Next, the c[4] value is checked and rounding is performed to 11 bits. Further, the MSB of the rounded 11 bits is checked, clipping is performed to prevent overflow, and the lower 10 bits are output. Note that since the coefficient has 8 bits and the 5th bit of the arithmetic results is rounded, the maximum gain by this operation is 255/32 = 7.96875 times and this can be varied in 256 steps. The arithmetic coefficient is shared by R, G and B, and the initial value is 020h.

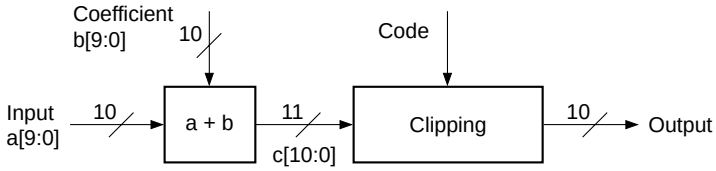


(b) User bright block

This block performs addition and subtraction processing as the user bright adjustment. The 10 bits of data a[9:0] output from the user gain block, a 10-bit coefficient b[9:0], and a 1-bit code are used as the inputs to perform arithmetic processing with an accuracy of 1 bit. Addition is performed when the code = 0, and subtraction when the code = 1. However, when performing subtraction, set an arithmetic coefficient that is the twos complement of the number to be subtracted.
The initial adder performs the following addition:

$$c[10:0] = a[9:0] + b[9:0]$$

Then, overflow and underflow are judged according to c[10] which is the MSB of the arithmetic results and the code data value. 3FFh is output when overflow occurs, and 000h when underflow occurs. Note that the arithmetic coefficient and code are shared by R, G and B, and the initial values are 000h and 0h, respectively.

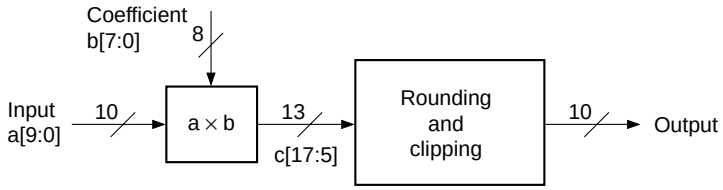


(c) Sub gain block

This block performs multiplication processing as the white balance gain adjustment. Multiplication is performed as follows using the 10-bit data a[9:0] output from the user bright block and an 8-bit coefficient b[7:0] as inputs.

$$c[17:0] = a[9:0] \times b[7:0]$$

The upper 13 bits c[17:5] of the arithmetic results are output. Next, the c[5] value is checked and rounding is performed to 12 bits. Further, the upper 2 bits of the rounded 12 bits are checked, clipping is performed to prevent overflow, and the lower 10 bits are output. Note that since the coefficient has 8 bits and the 6th bit of the arithmetic results is rounded, the maximum gain by this operation is 255/64 = 3.984375 times and this can be varied in 256 steps. The arithmetic coefficients can be set independently for R, G and B, and the initial value is 040h for each.

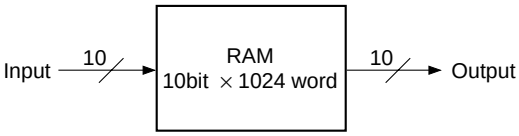


(d) Sub bright block

This block performs addition and subtraction processing as the white balance bright adjustment. Note that the block configuration is the same as the user bright block. However, the arithmetic coefficients and codes can be set independently for R, G and B, and the initial values are 000h and 0h for each, respectively.

(e) Gamma block

This block performs gamma correction for the user- and white balance-adjusted signal. This block comprises a 10-bit × 1024-word RAM, and the gamma correction curve can be set as desired. The results of this correction are output as 10 bits. The RAM data is set through the parallel I/F block. Note that the RAM output is undetermined while data is being set in this RAM, and also during power-on.

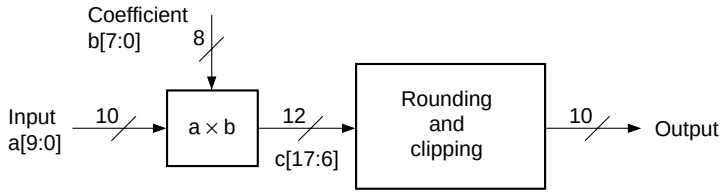


(f) Gamma gain block

This block performs multiplication processing for the gamma-corrected signal as the gain adjustment for correcting variance in the VT curve of the LCD panel. Multiplication is performed as follows using the 10-bit data a[9:0] output from the gamma block and an 8-bit coefficient b[7:0] as inputs.

$$c[17:0] = a[9:0] \times b[7:0]$$

The upper 12 bits c[17:6] of the arithmetic results are output. Next, the c[6] value is checked and rounding is performed to 11 bits. Further, the MSB of the rounded 11 bits is checked, clipping is performed to prevent overflow, and the lower 10 bits are output. Note that since the coefficient has 8 bits and the 7th bit of the arithmetic results is rounded, the maximum gain by this operation is 255/128 = 1.9921875 times and this can be varied in 256 steps. The arithmetic coefficients can be set independently for R, G and B, and the initial value is 080h for each.



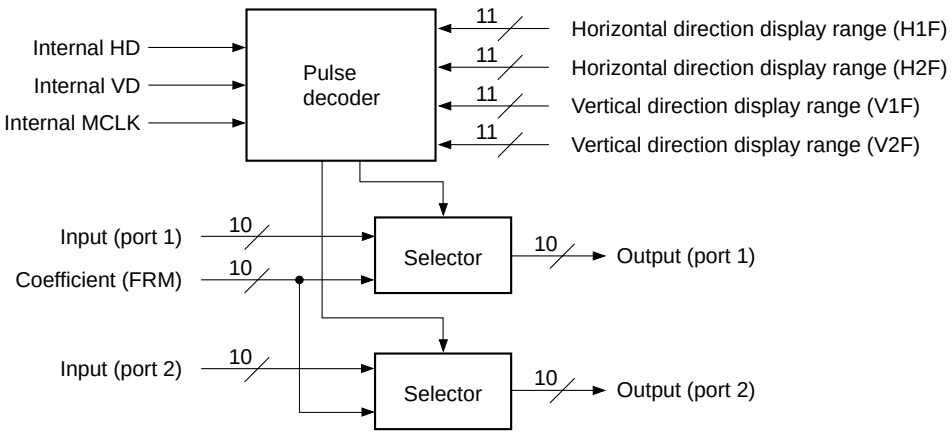
(g) Gamma bright block

This block performs addition and subtraction processing for the gamma-corrected signal as the bright adjustment for correcting variance in the VT curve of the LCD panel. Note that the block configuration is the same as the user bright block. However, the arithmetic coefficients and codes can be set independently for R, G and B, and the initial values are 000h and 0h for each, respectively.

(h) Black frame block

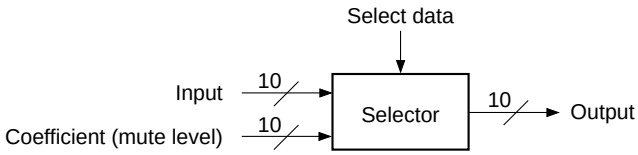
This block can perform processing to fix the blanking period of the video signal to the desired level regardless of the front-end signal processing results. This is effective when attempting to display a video signal which has been pixel-converted using a scan converter, etc., on a LCD panel or other display with a fixed number of pixels. If the number of pixels calculated from the effective period of the video signal to be displayed is less than the number of pixels of the display on which the signal is to be displayed, the blanking period of the video signal is displayed in the excess pixels. At this time, the displayed blanking period can be fixed to the desired level regardless of the gain and bright adjustment, gamma correction or other picture quality adjustment results by processing with this block.

Here, the desired range of the video signal is replaced with 10-bit data (FRM) by switching the video signal (port 1 and port 2) and the coefficients using the pulse output from the pulse decoder. This range can be set as desired by the 11-bit coefficients (H1F, H2F, V1F and V2F) set in the pulse decoder. Then separate pulses are output from the pulse decoder for each of the port 1 (R1, G1 and B1) and port 2 (R2, G2 and B2) processing system blocks. By doing so, the black frame display range can be controlled in 1-dot units for the horizontal direction and in 1-line units for the vertical direction. Note that the 1-dot unit for the horizontal direction is the 1-dot unit when viewed with the video signal displayed. Also, all coefficients are shared by R, G and B, and the initial value is 000h for each. However, note that when all black frame display range coefficients (H1F, H2F, V1F and V2F) are 000h, black frame display processing is not performed regardless of the black frame signal level coefficient values.



(i) Mute block

This block performs mute processing by replacing the video signal with data of the desired level. Of the arithmetic coefficients set from the register, the mute data can be set independently for R, G and B, and the initial value is 000h for each. Also, the mute processing select data is shared by R, G and B, and the initial value is 1h. Therefore, mute is applied in the initial status. This is because the gamma block RAM output value is undetermined in the initial status. Therefore, note that in order to output the video signal, the mute processing select data must be set to 0h after data is set in the RAM.

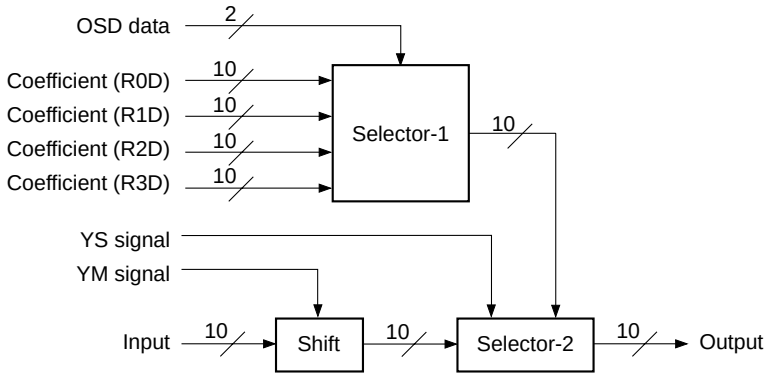


(j) OSD block

This block performs video signal half-tone processing and OSD-MIX processing by inputting the 2-bit OSD data for each color and the YS and YM signals. In the initial shift block, the input data is shifted by one bit to the LSB side when the YM signal is high level. For example, when 0F0h is input, 078h is output. Video signal half-tone processing is performed in this manner by halving the input data level.

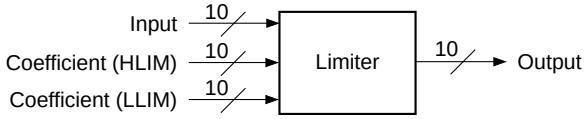
The selector-1 block determines the OSD level by assigning four types of coefficients with respect to the OSD input data. In the Red block, R0D is selected and output when the OSD data is 0h, R1D when 1h, R2D when 2h, and R3D when 3h. Similarly, one of G0D, G1D, G2D or G3D is selected in the Green block, and one of B0D, B1D, B2D or B3D in the Blue block. Next, the selector-2 block performs OSD-MIX processing by switching the video signal and the data selected by the selector-1 block using the YS signal. Here, the selector-1 block output data is selected and OSD-MIX processing is performed when the YS signal is high level.

The four coefficients can be set independently for R, G and B, and the initial values are all 000h. These coefficients are all 10 bits, and the OSD data is 2 bits for each of R, G and B, so 4 half tones can be selected as desired from among 1024 half tones for each of R, G and B. Therefore, the desired 64 (= 2^6) colors can be selected from among the total 1.07374 billion (= 2^{30}) colors for R, G and B.



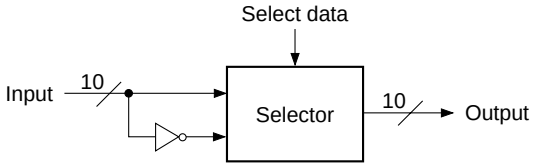
(k) Limiter block

This block performs limiter processing so that the output signal does not exceed a certain range. First, the input data is compared with the low-side limiter level LLIM and high-side limiter level HLIM coefficients. When these results are input data ≤ LLIM, the output is clipped at the LLIM level. When HLIM ≤ input data, the output is clipped at the HLIM level. When LLIM < IN < HLIM, the input data is output directly. Note that the two coefficients are shared by R, G and B, and the initial values are both 000h. Set the two coefficients so as to constantly maintain the relationship LLIM < HLIM. Also, when both coefficient values are 000h, limiter processing is not performed.



(l) Negative/positive inversion

This block performs negative/positive inversion processing. Here, negative/positive inversion processing is performed by outputting the input data directly when the select data is low, or inverting and outputting the input data when the select data is high. The select data is shared by R, G and B, and the initial value is 0h.



2. IRACT Block

The IRACT block consists of frequency divider and pulse generation circuits, and outputs a pulse synchronized with the horizontal sync signal input to HDIN2 from IRACT (Pin 164). The structure of this block is independent from other blocks in the CXD2467AQ. The clock system is also independent, so the IRACT block can be operated using a different clock than the TG and DSD blocks.

(a) Sync signal input pin and signal polarity switching pin (HDIN2 and HDPOL2)

The horizontal sync signal for the IRACT block is input to HDIN2 (Pin 38), and the sync signal polarity is set by HDPOL2 (Pin 39). Set HDPOL2 to high level when the horizontal sync signal is positive polarity, and to low level when negative polarity.

(b) Clock input pins (CLK3P/CLK3N, CLK3C and CLK4) and clock selection pins (CLKSEL3 and CLKSEL4)

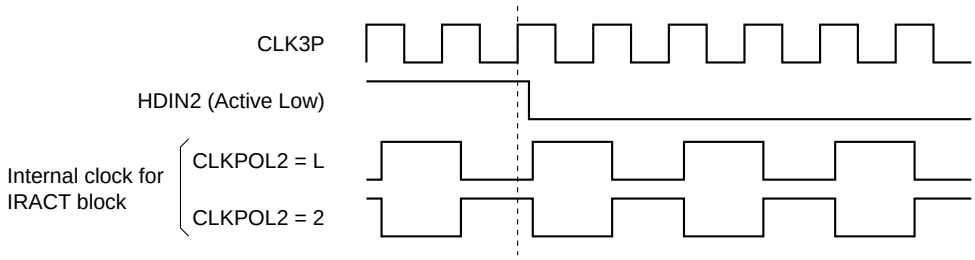
These are the clock input pins for the IRACT block. Like the master clock, a clock synchronized to the horizontal sync signal is input. The 1/N (N is the number of clocks during one horizontal period) frequency-divided clock pulse is output from IRRET (Pin 50). Like the master clock, the clock input pins consist of CLK3P/CLK3N (Pins 40 and 41) for small-amplitude differential input (center level: 2.0V, amplitude: ±0.4V), and CLK3C (Pin 44) and CLK4 (Pin 46) for CMOS level input for a total of three channels. These are selected according to CLKSEL3 (Pin 47) and CLKSEL4 (Pin 48).

CLKSEL3	CLKSEL4	Selected clock input pins
L	L	CLK3P/CLK3N (small-amplitude differential input, input at the same frequency as the dot clock)
H	L	CLK3C (CMOS level input, input at the same frequency as the dot clock)
—	H	CLK4 (CMOS level input, input at 1/2 the frequency of the dot clock)

—: Don't care

(c) Clock polarity switching pin (CLKPOL2)

When CLK3P/3N or CLK3C is selected, the clock is 1/2 frequency divided inside the IC using the falling edge of the HD pulse as the reference. The polarity of this 1/2 frequency-divided clock is switched by CLKPOL2 (Pin 49). Normally CLKPOL2 is used at low level.



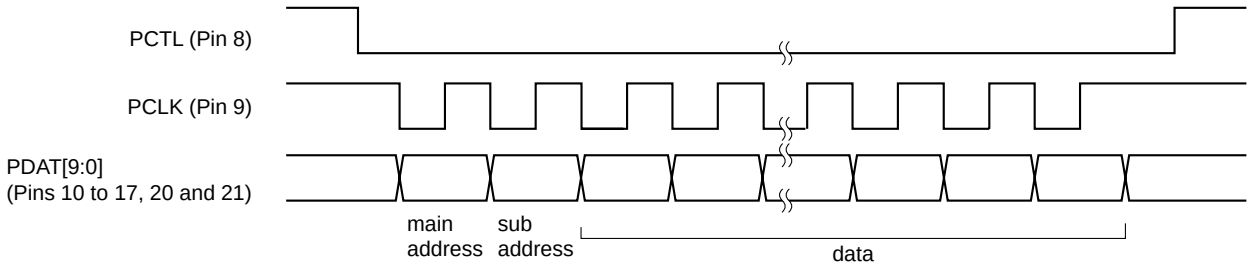
3. System Clear Pin (XCLR)

All internal circuits are initialized by setting XCLR (Pin 53) low. Initialization should be performed during power-on.

4. Parallel I/F Block

Register data settings in this IC are performed by parallel data. As shown in the Timing Chart below, the parallel I/F comprises a total 12-bit wide bus consisting of control signal PCTL (Pin 8), clock signal PCLK (Pin 9) and 10-bit wide data signal PDAT[9:0] (Pins 10 to 17, 20 and 21).
The data signal is input in the order of main address, sub address and data. When setting data in this IC, divide the data into five blocks as shown in the table below. Next, the sub address specifies the initial address of the data to be written in the block designated by the main address. The data is set sequentially from the data at the address designated by the sub address. The address of each data set thereafter is automatically incremented by +1 from the address designated by the sub address, so further address setting is unnecessary. This makes it possible to set only the necessary data from the desired address of the desired block.

Timing Chart



Main Address Table

Main address	Set block
000h	Gamma block (Red) RAM
001h	Gamma block (Green) RAM
002h	Gamma block (Blue) RAM
003h	DSD arithmetic coefficients for other than gamma block
004h	TG and IRACT block setting data

4-1. Gamma Block (Main Address: 000h to 002h)

In this block, the gamma correction data is set in a 10-bit × 1024-word RAM. Here, the set sub address directly becomes the RAM write address. Thereafter, the RAM write address is automatically incremented by +1. Following the main address, designate the RAM write start address in the sub address with 10 bits, then set the gamma correction data in 10 bits.

4-2. DSD Block (Main Address: 003h)

The DSD block data format is as follows.

Data Format

Sub address	Data										Initial value
	PDAT9	PDAT8	PDAT7	PDAT6	PDAT5	PDAT4	PDAT3	PDAT2	PDAT1	PDAT0	
000h	—	UBF	UG7	UG6	UG5	UG4	UG3	UG2	UG1	UG0	020h
001h	UB9	UB8	UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0	000h
002h	—	RSBF	RSG7	RSG6	RSG5	RSG4	RSG3	RSG2	RSG1	RSG0	040h
003h	RSB9	RSB8	RSB7	RSB6	RSB5	RSB4	RSB3	RSB2	RSB1	RSB0	000h
004h	—	GSBF	GSG7	GSG6	GSG5	GSG4	GSG3	GSG2	GSG1	GSG0	040h
005h	GSB9	GSB8	GSB7	GSB6	GSB5	GSB4	GSB3	GSB2	GSB1	GSB0	000h
006h	—	BSBF	BSG7	BSG6	BSG5	BSG4	BSG3	BSG2	BSG1	BSG0	040h
007h	BSB9	BSB8	BSB7	BSB6	BSB5	BSB4	BSB3	BSB2	BSB1	BSB0	000h
008h	—	RGBF	RGG7	RGG6	RGG5	RGG4	RGG3	RGG2	RGG1	RGG0	080h
009h	RGB9	RGB8	RGB7	RGB6	RGB5	RGB4	RGB3	RGB2	RGB1	RGB0	000h
00Ah	—	GGBF	GGG7	GGG6	GGG5	GGG4	GGG3	GGG2	GGG1	GGG0	080h
00Bh	GGB9	GGB8	GGB7	GGB6	GGB5	GGB4	GGB3	GGB2	GGB1	GGB0	000h
00Ch	—	BGBF	BGG7	BGG6	BGG5	BGG4	BGG3	BGG2	BGG1	BGG0	080h
00Dh	BGB9	BGB8	BGB7	BGB6	BGB5	BGB4	BGB3	BGB2	BGB1	BGB0	000h
00Eh	FRM9	FRM8	FRM7	FRM6	FRM5	FRM4	FRM3	FRM2	FRM1	FRM0	000h
00Fh	H1F9	H1F8	H1F7	H1F6	H1F5	H1F4	H1F3	H1F2	H1F1	H1F0	000h
010h	—	—	—	—	—	—	—	—	—	H1F10	000h
011h	H2F9	H2F8	H2F7	H2F6	H2F5	H2F4	H2F3	H2F2	H2F1	H2F0	000h
012h	—	—	—	—	—	—	—	—	—	H2F10	000h
013h	V1F9	V1F8	V1F7	V1F6	V1F5	V1F4	V1F3	V1F2	V1F1	V1F0	000h
014h	—	—	—	—	—	—	—	—	—	V1F10	000h
015h	V2F9	V2F8	V2F7	V2F6	V2F5	V2F4	V2F3	V2F2	V2F1	V2F0	000h
016h	—	—	—	—	—	—	—	SMSEL	INVSEL	V2F10	004h
017h	RM9	RM8	RM7	RM6	RM5	RM4	RM3	RM2	RM1	RM0	000h
018h	GM9	GM8	GM7	GM6	GM5	GM4	GM3	GM2	GM1	GM0	000h
019h	BM9	BM8	BM7	BM6	BM5	BM4	BM3	BM2	BM1	BM0	000h
01Ah	R0D9	R0D8	R0D7	R0D6	R0D5	R0D4	R0D3	R0D2	R0D1	R0D0	000h
01Bh	R1D9	R1D8	R1D7	R1D6	R1D5	R1D4	R1D3	R1D2	R1D1	R1D0	000h
01Ch	R2D9	R2D8	R2D7	R2D6	R2D5	R2D4	R2D3	R2D2	R2D1	R2D0	000h
01Dh	R3D9	R3D8	R3D7	R3D6	R3D5	R3D4	R3D3	R3D2	R3D1	R3D0	000h
01Eh	G0D9	G0D8	G0D7	G0D6	G0D5	G0D4	G0D3	G0D2	G0D1	G0D0	000h
01Fh	G1D9	G1D8	G1D7	G1D6	G1D5	G1D4	G1D3	G1D2	G1D1	G1D0	000h
020h	G2D9	G2D8	G2D7	G2D6	G2D5	G2D4	G2D3	G2D2	G2D1	G2D0	000h
021h	G3D9	G3D8	G3D7	G3D6	G3D5	G3D4	G3D3	G3D2	G3D1	G3D0	000h
022h	B0D9	B0D8	B0D7	B0D6	B0D5	B0D4	B0D3	B0D2	B0D1	B0D0	000h
023h	B1D9	B1D8	B1D7	B1D6	B1D5	B1D4	B1D3	B1D2	B1D1	B1D0	000h
024h	B2D9	B2D8	B2D7	B2D6	B2D5	B2D4	B2D3	B2D2	B2D1	B2D0	000h
025h	B3D9	B3D8	B3D7	B3D6	B3D5	B3D4	B3D3	B3D2	B3D1	B3D0	000h
026h	LLIM9	LLIM8	LLIM7	LLIM6	LLIM5	LLIM4	LLIM3	LLIM2	LLIM1	LLIM0	000h
027h	HLIM9	HLIM8	HLIM7	HLIM6	HLIM5	HLIM4	HLIM3	HLIM2	HLIM1	HLIM0	000h

—: Don't care

The detailed setting contents are described below.

(a) UG: User gain block coefficient setting

The user gain block arithmetic coefficient is set in UG7 (MSB) to UG0 (LSB). The initial value is 20h.

(b) UB and UBF: User bright block coefficient settings

The user bright block arithmetic coefficient is set in UB9 (MSB) to UB0 (LSB), and the code bit is set in UBF. Addition is performed when the code bit = 0, and subtraction when the code bit = 1. When performing subtraction, set an arithmetic coefficient that is the twos complement of the number to be subtracted. The initial values of the arithmetic coefficient and the code bit are 000h and 0h, respectively.

(c) RSG, GSG and BSG: Sub gain block coefficient settings

The R, G and B sub gain block arithmetic coefficients are set in RSG7 (MSB) to RSG0 (LSB), GSG7 (MSB) to GSG0 (LSB) and BSG7 (MSB) to BSG0 (LSB), respectively. The initial value of each coefficient is 40h.

(d) RSB, RSBF, GSB, GSBF, BSB and BSBF: Sub bright block coefficient settings

The R, G and B sub bright block arithmetic coefficients are set in RSB9 (MSB) to RSB0 (LSB), GSB9 (MSB) to GSB0 (LSB) and BSB9 (MSB) to BSB0 (LSB), respectively. Also, the R, G and B code bits are set in RSBF, GSBF and BSBF, respectively. Addition is performed when the code bit = 0, and subtraction when the code bit = 1. When performing subtraction, set an arithmetic coefficient that is the twos complement of the number to be subtracted. The initial values of the arithmetic coefficients and the code bits are 000h and 0h, respectively.

(e) RGG, GGG and BGG: Gamma gain block coefficient settings

The R, G and B gamma gain block arithmetic coefficients are set in RGG7 (MSB) to RGG0 (LSB), GGG7 (MSB) to GGG0 (LSB) and BGG7 (MSB) to BGG0 (LSB), respectively. The initial value of each coefficient is 80h.

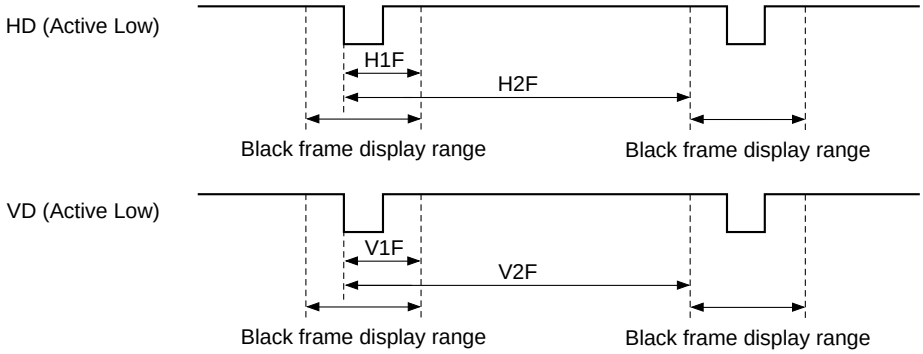
(f) RGB, RGBF, GGB, GGBF, BGB and BGBF: Gamma bright block coefficient settings

The R, G and B gamma bright block arithmetic coefficients are set in RGB9 (MSB) to RGB0 (LSB), GGB9 (MSB) to GGB0 (LSB) and BGB9 (MSB) to BGB0 (LSB), respectively. Also, the R, G and B code bits are set in RGBF, GGBF and BGBF, respectively. Addition is performed when the code bit = 0, and subtraction when the code bit = 1. When performing subtraction, set an arithmetic coefficient that is the twos complement of the number to be subtracted. The initial values of the arithmetic coefficients and the code bits are 000h and 0h, respectively.

(g) FRM, H1F, H2F, V1F and V2F: Black frame processing block coefficient settings

The black frame signal level for the black frame processing block is set in FRM9 (MSB) to FRM0 (LSB). In addition, the black frame display range coefficients for the horizontal direction are set in H1F10 (MSB) to H1F0 (LSB) and H2F10 (MSB) to H2F0 (LSB), and for the vertical direction in V1F10 (MSB) to V1F0 (LSB) and V2F10 (MSB) to V2F0 (LSB).

The horizontal direction display range can be set in 1-dot units using the HD input edge as the reference. The falling edge is used as the reference when HD input is negative polarity input, and the rising edge when positive polarity input. The vertical direction display range can be set in 1-line units using the VD input edge as the reference. The falling edge is used as the reference when VD input is negative polarity input, and the rising edge when positive polarity input. Set the display range values in H1F , H2F, V1F and V2F. Note that when all black frame display range coefficients are 000h, black frame processing is not performed. The initial value of each coefficient is 000h.



(h) SMSEL, RM, GM and BM: Mute block coefficient settings

The mute processing select data for the R, G and B mute blocks is set in SMSEL. Also, the R, G and B mute level coefficients are set in RM9 (MSB) to RM0 (LSB), GM9 (MSB) to GM0 (LSB) and BM9 (MSB) to BM0 (LSB), respectively. Mute processing is performed when SMSEL = 1, and not when SMSEL = 0. The initial values of the select data and mute level coefficients are 1h and 000h, respectively.

(i) R0D, R1D, R2D, R3D, G0D, G1D, G2D, G3D, B0D, B1D, B2D and B3D: OSD block coefficient settings

The R, G and B OSD block decoding data is set in R0D9 (MSB) to R0D0 (LSB), R1D9 (MSB) to R1D0 (LSB), R2D9 (MSB) to R2D0 (LSB), R3D9 (MSB) to R3D0 (LSB), G0D9 (MSB) to G0D0 (LSB), G1D9 (MSB) to G1D0 (LSB), G2D9 (MSB) to G2D0 (LSB), G3D9 (MSB) to G3D0 (LSB), B0D9 (MSB) to B0D0 (LSB), B1D9 (MSB) to B1D0 (LSB), B2D9 (MSB) to B2D0 (LSB) and B3D9 (MSB) to B3D0 (LSB). The desired OSD color can be set by assigning the decoding data with respect to the input OSD data in the OSD block. The initial values are all 000h.

(j) LLIM, HLIM: Limiter block coefficient settings

The limiter block limit value data is set in LLIM9 (MSB) to LLIM0 (LSB) and HLIM9 (MSB) to HLIM0 (LSB). Be sure to set data so that the relationship LLIM < HLIM is constantly maintained. Note that when 000h is set for both LLIM and HLIM, limiter processing is not performed. The initial values are both 000h.

(k) INVSEL: Negative/positive inversion block coefficient setting

The negative/positive inversion block select data is set in INVSEL. Negative/positive inversion processing is performed when INVSEL = 1, and not when INVSEL = 0. The initial value is 0h, respectively.

4-3. TG and IRACT Blocks (Main Address: 004h)

The timing pulses output from the CXD2467AQ are generated according to the data set in the data register. The related registers are shown below. Sub addresses 000h to 025h are the TG block related data, and 026h to 02Bh are the IRACT block related data. The TG and IRACT block data format is as follows.

Data Format

Sub address	Data										Initial value
	PDAT9	PDAT8	PDAT7	PDAT6	PDAT5	PDAT4	PDAT3	PDAT2	PDAT1	PDAT0	
000h	PLP9	PLP8	PLP7	PLP6	PLP5	PLP4	PLP3	PLP2	PLP1	PLP0	297h
001h	—	SLVRS	SLPRS3	SLPRS2	SLPRS1	SLPRS0	SLHCK1	SLHCK0	PLP11	PLP10	015h
002h	ORU9	ORU8	ORU7	ORU6	ORU5	ORU4	ORU3	ORU2	ORU1	ORU0	080h
003h	—	—	—	—	—	—	—	—	ORU11	ORU10	000h
004h	ORD9	ORD8	ORD7	ORD6	ORD5	ORD4	ORD3	ORD2	ORD1	ORD0	000h
005h	—	—	—	—	—	—	—	—	ORD11	ORD10	000h
006h	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	022h
007h	—	—	—	—	—	—	—	—	HP11	HP10	000h
008h	PCGU9	PCGU8	PCGU7	PCGU6	PCGU5	PCGU4	PCGU3	PCGU2	PCGU1	PCGU0	086h
009h	—	—	—	—	—	—	—	—	PCGU11	PCGU10	000h
00Ah	PCGD9	PCGD8	PCGD7	PCGD6	PCGD5	PCGD4	PCGD3	PCGD2	PCGD1	PCGD0	142h
00Bh	—	—	—	—	—	—	—	—	PCGD11	PCGD10	000h
00Ch	PRGU9	PRGU8	PRGU7	PRGU6	PRGU5	PRGU4	PRGU3	PRGU2	PRGU1	PRGU0	086h
00Dh	—	—	—	—	—	—	—	—	PRGU11	PRGU10	000h
00Eh	PRGD9	PRGD8	PRGD7	PRGD6	PRGD5	PRGD4	PRGD3	PRGD2	PRGD1	PRGD0	100h
00Fh	—	—	—	—	—	—	—	—	PRGD11	PRGD10	000h
010h	ENBU9	ENBU8	ENBU7	ENBU6	ENBU5	ENBU4	ENBU3	ENBU2	ENBU1	ENBU0	0FEh
011h	—	—	—	—	—	—	—	—	ENBU11	ENBU10	000h
012h	ENBD9	ENBD8	ENBD7	ENBD6	ENBD5	ENBD4	ENBD3	ENBD2	ENBD1	ENBD0	00Ch
013h	—	—	—	—	—	—	—	—	ENBD11	ENBD10	000h
014h	CP1U9	CP1U8	CP1U7	CP1U6	CP1U5	CP1U4	CP1U3	CP1U2	CP1U1	CP1U0	0C0h
015h	—	—	—	—	—	—	—	—	CP1U11	CP1U10	000h
016h	CP1D9	CP1D8	CP1D7	CP1D6	CP1D5	CP1D4	CP1D3	CP1D2	CP1D1	CP1D0	132h
017h	—	—	—	—	—	—	—	—	CP1D11	CP1D10	000h
018h	CP2U9	CP2U8	CP2U7	CP2U6	CP2U5	CP2U4	CP2U3	CP2U2	CP2U1	CP2U0	088h
019h	—	—	—	—	—	—	—	—	CP2U11	CP2U10	000h
01Ah	CP2D9	CP2D8	CP2D7	CP2D6	CP2D5	CP2D4	CP2D3	CP2D2	CP2D1	CP2D0	128h
01Bh	—	—	—	—	—	—	—	—	CP2D11	CP2D10	000h
01Ch	HSTU9	HSTU8	HSTU7	HSTU6	HSTU5	HSTU4	HSTU3	HSTU2	HSTU1	HSTU0	146h
01Dh	—	—	—	—	—	—	—	—	HSTU11	HSTU10	000h
01Eh	HSTD9	HSTD8	HSTD7	HSTD6	HSTD5	HSTD4	HSTD3	HSTD2	HSTD1	HSTD0	15Eh
01Fh	—	—	—	—	—	—	—	—	HSTD11	HSTD10	000h
020h	VCRV9	VCRV8	VCRV7	VCRV6	VCRV5	VCRV4	VCRV3	VCRV2	VCRV1	VCRV0	086h
021h	—	—	—	—	—	—	—	—	VCRV11	VCRV10	000h
022h	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	020h
023h	—	—	—	SLFR	HSCN	VSCN	HB	VB1	VB2	VP10	02Eh
024h	FRI9	FRI8	FRI7	FRI6	FRI5	FRI4	FRI3	FRI2	FRI1	FRI0	3FFh
025h	—	SLDS	MBK1	MBK0	SHP0	SHP1	SHP2	SHP3	INV	FRI10	001h
026h	IRP9	IRP8	IRP7	IRP6	IRP5	IRP4	IRP3	IRP2	IRP1	IRP0	297h
027h	—	—	—	—	—	—	—	SLHR	IRP11	IRP10	001h
028h	IRU9	IRU8	IRU7	IRU6	IRU5	IRU4	IRU3	IRU2	IRU1	IRU0	080h
029h	—	—	—	—	—	—	—	—	IRU11	IRU10	000h
02Ah	IRD9	IRD8	IRD7	IRD6	IRD5	IRD4	IRD3	IRD2	IRD1	IRD0	000h
02Bh	—	—	—	—	—	—	—	—	IRD11	IRD10	000h

—: Don't care

The detailed setting contents are described below.

(a) PLP: PLL counter frequency division ratio setting

This sets the frequency division ratio of the 1/N frequency divider (PLL counter) for phase comparison. The value of (total number of dots in one horizontal period N) – 1 is set in PLP11 (MSB) to PLP0 (LSB). The frequency division ratio can be set up to 4096. However, only even numbers can be set for the value of N. The initial value is 697h (N = 1688).

(b) SLHCK: HCK cycle setting

The HCK1 (Pin 142) and HCK2 (Pin 143) cycle is set in SLHCK1 (MSB) and SLHCK0 (LSB). 0h is set for LCD panels that perform 6-dot simultaneous sampling, 1h for 12-dot simultaneous sampling, 2h for 18-dot simultaneous sampling and 3h for 24-dot simultaneous sampling. Note that HCK2 is the reverse-phase signal of HCK1. The initial value is 1h (12-dot simultaneous sampling).

(c) SLPRS: PLL counter reset cycle setting

The PLL counter is reset according to the value set in PLP, but reset can also be applied separately by HSYNC. The HSYNC cycle at which reset is applied is set in SLPRS3 (MSB) to SLPRS0 (LSB). When 0h is set, the PLL counter is not reset. When 1h is set, the front edge of HSYNC is detected and the PLL counter is reset each time HSYNC is input. The reset cycle increases thereafter so that when Fh is set, the PLL counter is reset by HSYNC every 15H. The initial value is 1h (reset every 1H).

(d) SLVRS: PLL counter VSYNC reset

This sets whether to reset the PLL counter with each VSYNC. The PLL counter is not reset when set to 0h, and reset when 1h. However, when SLPRS = 0h (no reset by HSYNC), the PLL counter is not reset regardless of the SLVRS setting. The initial value is 0h (no reset).

(e) ORU/ORD: ORACT pulse settings

The ORACT (Pin 165) pulse rise position within one horizontal period is set in ORU11 (MSB) to ORU0 (LSB), and the fall position is set in ORD11 (MSB) to ORD0 (LSB). The PLL counter reset timing is used as the reference (all 0). Also, the least significant bit is ignored, so setting is in 2-dot units. The initial values are ORU = 080h and ORD = 000h.

(f) HP: Picture horizontal position setting

The timing at which the counter is initialized to generate the PCG (Pin 130), PRG (Pin 154), ENB (Pin 140), CLP1 (Pin 155), CLP2 (Pin 156), HST (Pin 149), HCK1 and HCK2 horizontal drive pulses within one horizontal period is set in HP11 (MSB) to HP0 (LSB). Changing this setting causes the phase relationships of the horizontal drive pulses as well as the changing positions of VCK (Pin 137) and FRP (Pin 153) relative to HSYNC to change in an interlocked manner, making it possible to change the picture horizontal position. Settings can be made in 1-dot units. Note that HCK1 and HCK2 are initialized at this timing, and change at the cycle set by SLHCK. (See the Timing Chart.) The initial value is 022h.

(g) PCGU/PCGD, PRGU/PRGD, ENBU/ENBD, CP1U/CP1D, CP2U/CP2D and HSTU/HSTD: Horizontal drive pulse settings

These set the rise and fall positions of the PCG, PRG, ENB, CLP1, CLP2 and HST pulses within one horizontal period. The horizontal drive pulse initialization timing set by HP is used as the reference. (See the Timing Chart.) Also, the least significant bit is ignored, so setting is in 2-dot units. The initial values are as follows.

PCGU = 086h/PCGD = 142h
PRGU = 086h/PRGD = 100h
ENBU = 0FEh/ENBD = 00Ch
CP1U = 0C0h/CP1D = 132h
CP2U = 088h/CP2D = 128h
HSTU = 146h/HSTD = 15Eh

(h) VCRV: VCK pulse polarity inversion position setting

The VCK and FRP pulse polarity inversion position within one horizontal period is set in VCRV11 (MSB) to VCRV0 (LSB). The reference is the same as that for the horizontal drive pulse setting above. Also, the least significant bit is ignored, so setting is in 2-dot units. The initial value is 086h.

(i) VP: Picture vertical position setting

The picture vertical position is set in VP10 (MSB) to VP0 (LSB). Changing this setting causes the phase relationships of the VST (Pin 136), VCK and FRP pulses relative to VSYNC to change in an interlocked manner. Settings can be made in 1-line units. The initial value is 020h.

(j) HB, VB1 and VB2: LCD panel control signal settings

These set the LCD panel control signals. The data set in HB, VB1 and VB2 is output from the HB (Pin 134), VB1 (Pin 132) and VB2 (Pin 131) output pins, respectively. Also, when either VB1 or VB2 is set to 0h, the BLK pulse is output. The methods of using these signals differ according to the LCD panel, and some LCD panels may not even have input pins supporting these signals. See the specifications of the used LCD panel for details. The initial values are HB = 1h, VB1 = 1h and VB2 = 1h.

(k) HSCN and VSCN: LCD panel scan direction settings

These set the horizontal and vertical scan directions of the LCD panel. The HSCN setting data is output from RGT (Pin 151), and the VSCN setting data from DWN (Pin 135). Also, changing the HSCN setting reverses the HCK1 and HCK2 phases. See the specifications of the used LCD panel for a detailed description of the scan direction. The initial values are HSCN = 1h and VSCN = 0h.

(l) SLFR: FRP pulse inversion cycle setting

This sets the inversion cycle of the polarity inversion pulse (FRP pulse) used for AC driving of LCD panels. The polarity is inverted at 1-line cycles when set to 0h, and at 1-field cycles when set to 1h. The initial value is 0h (1-line inversion).

(m) SHP0, SHP1, SHP2, SHP3 and INV: CXA2112R sample-and-hold control

These control the sample-and-hold position of the CXA2112R (sample-and-hold driver). The SHP0, SHP1, SHP2 and SHP3 setting data is reflected to SHA, SHB, SHC and SHD (Pins 157 to 160) as shown below. Also, the INV setting data is output directly from the INV (Pin 161) output pin. See the specifications of the CXA2112R for a detailed description of control methods. The initial values are SHP0 = 0h, SHP1 = 0h, SHP2 = 0h, SHP3 = 0h and INV = 0h.

Setting	Output				Setting	Output			
SHP3 to SHP0	SHPA	SHPB	SHPC	SHPD	SHP3 to SHP0	SHPA	SHPB	SHPC	SHPD
0000	L	L	L	L	1000	L	L	Z	L
0001	H	H	L	L	1001	H	H	Z	L
0010	Z	L	L	L	1010	Z	L	Z	L
0011	Z	H	L	L	1011	Z	H	Z	L
0100	L	L	H	H	1100	L	L	Z	H
0101	H	H	H	H	1101	H	H	Z	H
0110	Z	L	H	H	1110	Z	L	Z	H
0111	Z	H	H	H	1111	Z	H	Z	H

Z: High impedance state

(n) FRI: Free-running cycle setting

When VSYNC has not been input for a specified period, a judgment of "no signal" is made to allow AC driving of LCD panels even when there is no signal. In this case, a vertical start pulse and FRP pulse are output at a specified cycle (free-running operation). The period until a judgment of "no signal" is made and the VST pulse cycle during free-running operation are set in FRI10 (MSB) to FRI0 (LSB). The initial value is 7FFh (2048H cycle).

(o) MBK0 and MBK1: Decimation operation settings

This sets the decimation operation which decimates the display lines at a specified ratio. This IC has two built-in modes: 2/14-line decimation and 1/4-line decimation. MBK0 turns decimation operation on and off, and MBK1 selects the mode. Decimation is not performed when MBK0 = 0h, and is performed when MBK0 = 1h. Also, 2/14-line decimation is performed when MBK1 = 0h, and 1/4-line decimation when MBK1 = 1h. The initial values are MBK0 = 0h and MBK1 = 0h (no decimation).

(p) SLDS: Test data

This is test data. Set to 0h. The initial value is 0h.

(q) IRP: IRACT block frequency divider frequency division ratio setting

Like the PLL counter, this sets the frequency division ratio of the 1/N frequency divider for phase comparison. The value of (total number of dots in one horizontal period N) – 1 is set in IRP11 (MSB) to IRP0 (LSB). The frequency division ratio can be set up to 4096. However, only even numbers can be set for the value of N. The initial value is 697h (N = 1688).

(r) SLHR: IRACT block frequency divider reset setting

This sets whether the IRACT block frequency divider is reset by the HSYNC input to HDIN2. The frequency divider is reset when 0h, and not reset when 1h. The initial value is 0h (reset).

(s) IRU/IRD: IRACT pulse settings

The IRACT pulse rise position within one horizontal period is set in IRU11 (MSB) to IRU0 (LSB), and the fall position in IRD11 (MSB) to IRD0 (LSB) relative to the HSYNC input to HDIN2. The IRACT block frequency divider reset timing is used as the reference (all 0). Also, the least significant bit is ignored, so setting is in 2-dot units. The initial values are IRU = 080h and IRD = 000h.

Note) The above setting values may be invalid in certain cases. (For example, settings which exceed the number of clocks in 1H or number of lines in 1V of the input signal, etc.) Normal pulses will not be output in these cases, so be sure to refer to the setting examples on the following page when making the settings.

Data Register Setting Examples

Examples of data register settings for typical LCD panels driven by this IC and input signals are shown below. The optimum settings may differ depending on the actual input signal specifications and differences in video signal processing systems, so be sure to adjust the setting values as necessary.

(a) Example settings when using the LCX028

Input signal: SXGA (1280 × 1024 dots, f_H = 64kHz, f_V = 60Hz, dot clock = 108MHz)

PLL counter	PLP = 697h (N = 1688, same as default value)
H position	HP = 000h
PCG pulse	PCGU = 074h/PCGD = 136h
PRG pulse	PRGU = 074h/PRGD = 0F6h
ENB pulse	ENBU = 0F6h/ENBD = 008h
CLP1 pulse	CP1U = 088h/CP1D = 128h
HST pulse	HSTU = 146h/HSTD = 15Eh
VCK/FRP inversion position	VCRV = 074h
V position	VP = 020h (same as default value)

(b) Example settings when using the LCX023 or LCX017

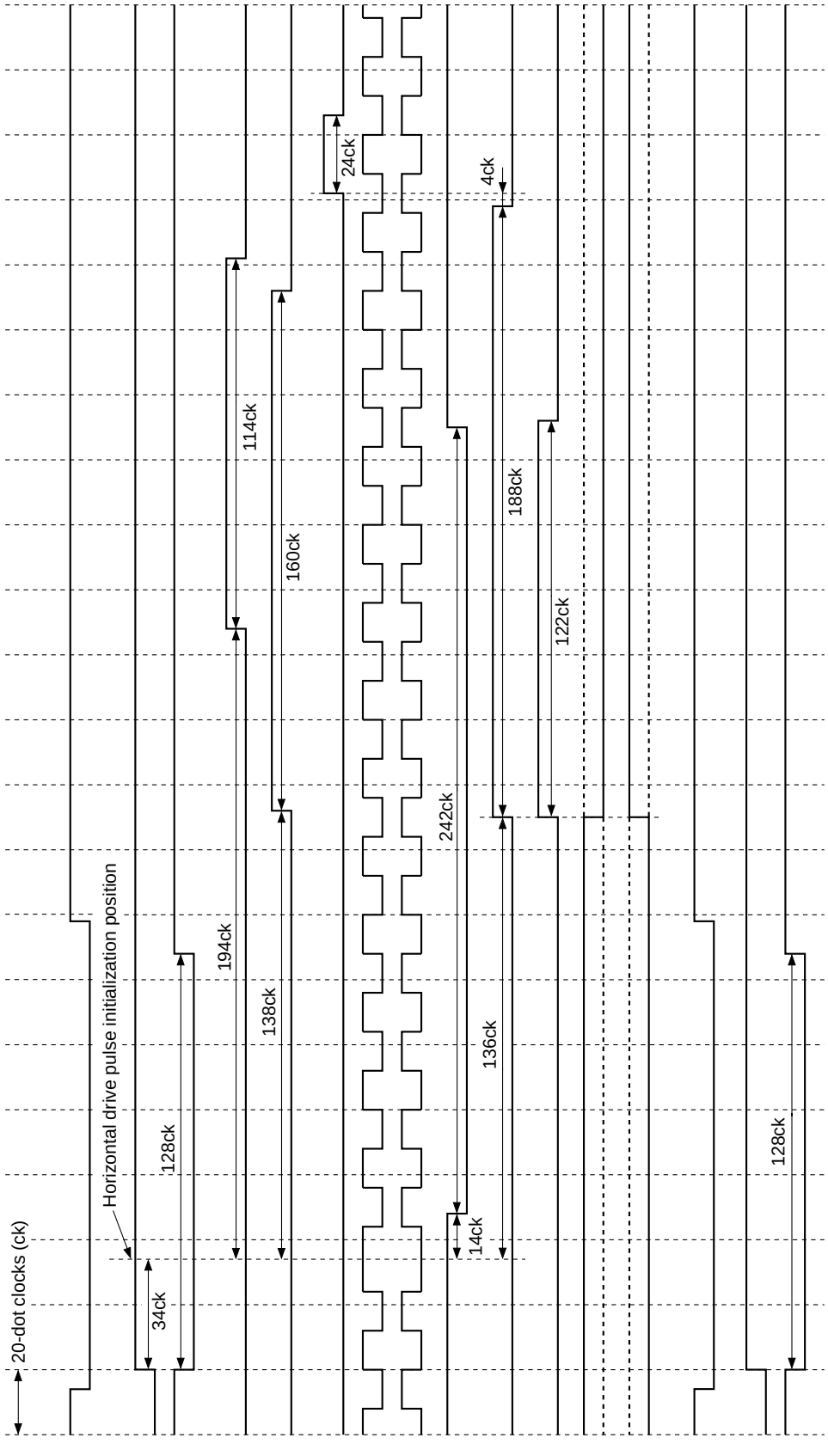
Input signal: XGA (1024 × 768 dots, f_H = 48kHz, f_V = 60Hz, dot clock = 65MHz)

PLL counter	PLP = 53Fh (N = 1344)
H position	HP = 042h
PCG pulse	PCGU = 050h/PCGD = 0D4h
PRG pulse	PRGU = 050h/PRGD = 09Eh
ENB pulse	ENBU = 09Eh/ENBD = 002h
CLP1 pulse	CP1U = 024h/CP1D = 0B0h
HST pulse	HSTU = 0CEh/HSTD = 0E6h
VCK/FRP inversion position	VCRV = 050h
V position	VP = 023h
Free-running frequency	FRI = 63Fh (1600H)

TG and IRACT Block Timing Chart

Horizontal Direction Timing Chart

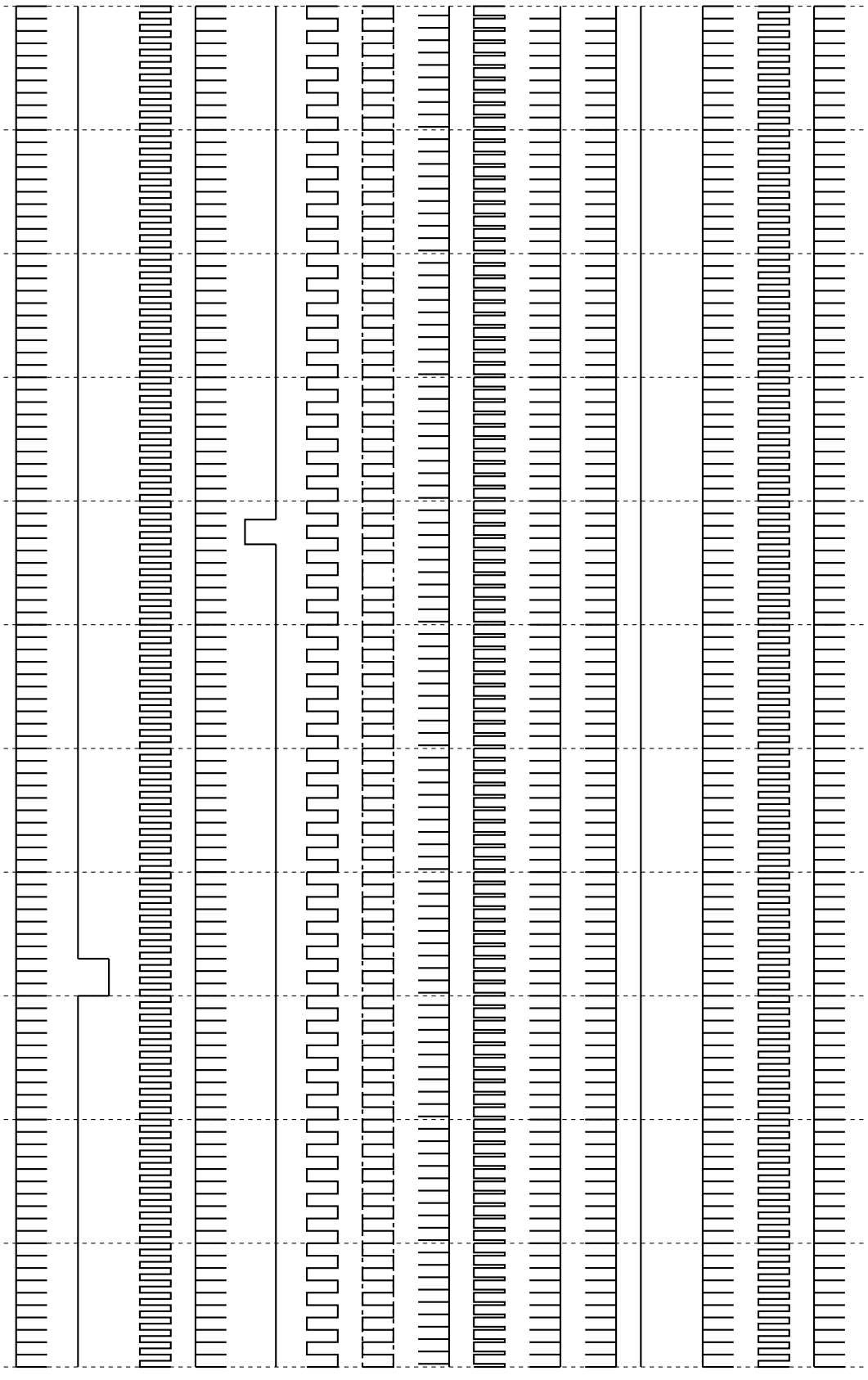
Data register setting: Default
(Example for input signal with total number of horizontal dots = 1688)



* When HSCN = 0 (left/right inversion), the HCK1 and HCK2 phases are reversed.
The 1H and 1V cycle FRP polarity is not specified.

Vertical Direction Timing Chart

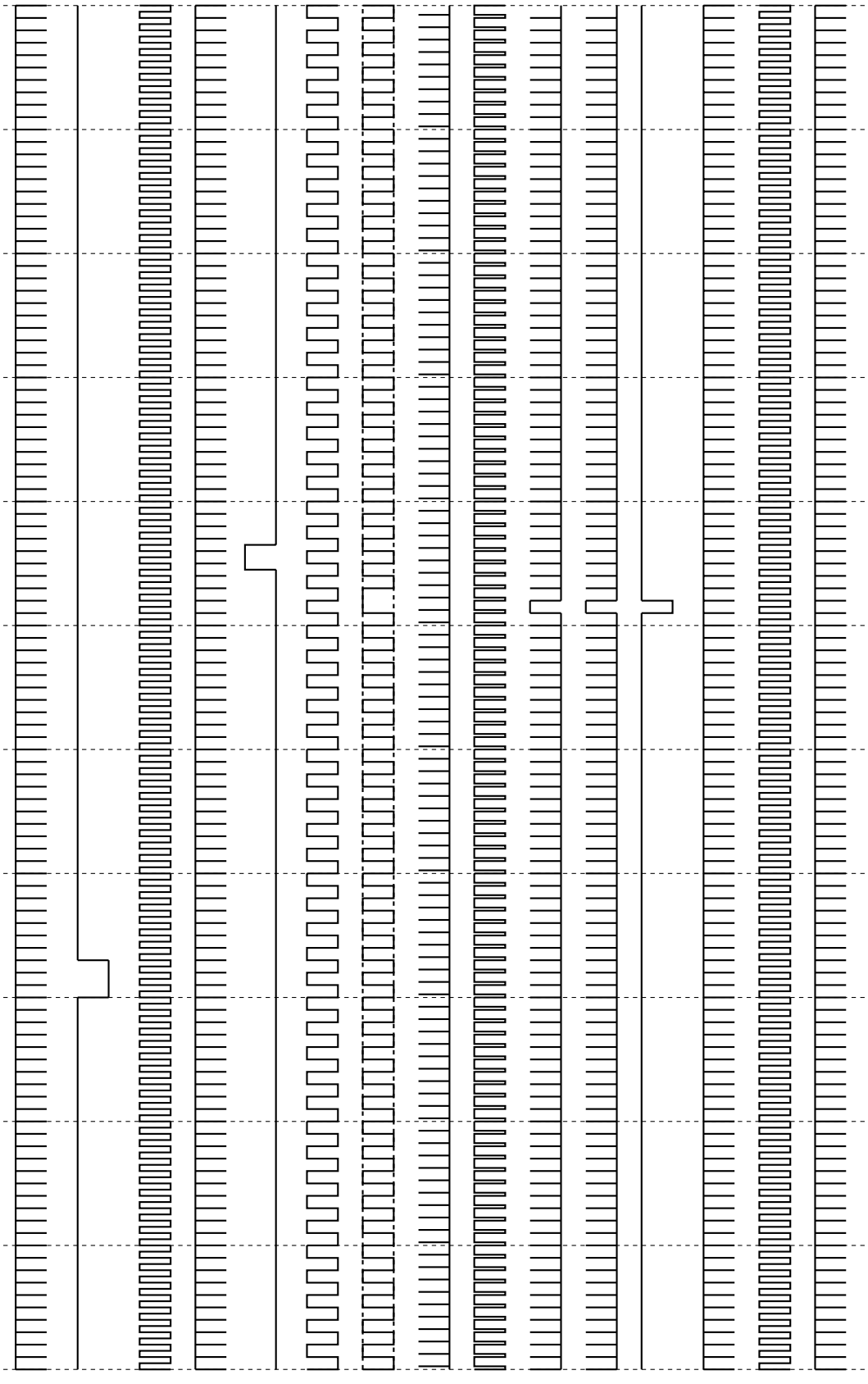
Data register setting: Default
(Example for input signal with total number of vertical lines = 1066)



* The 1H and 1V cycle FRP polarity is not specified.

Vertical Direction Timing Chart

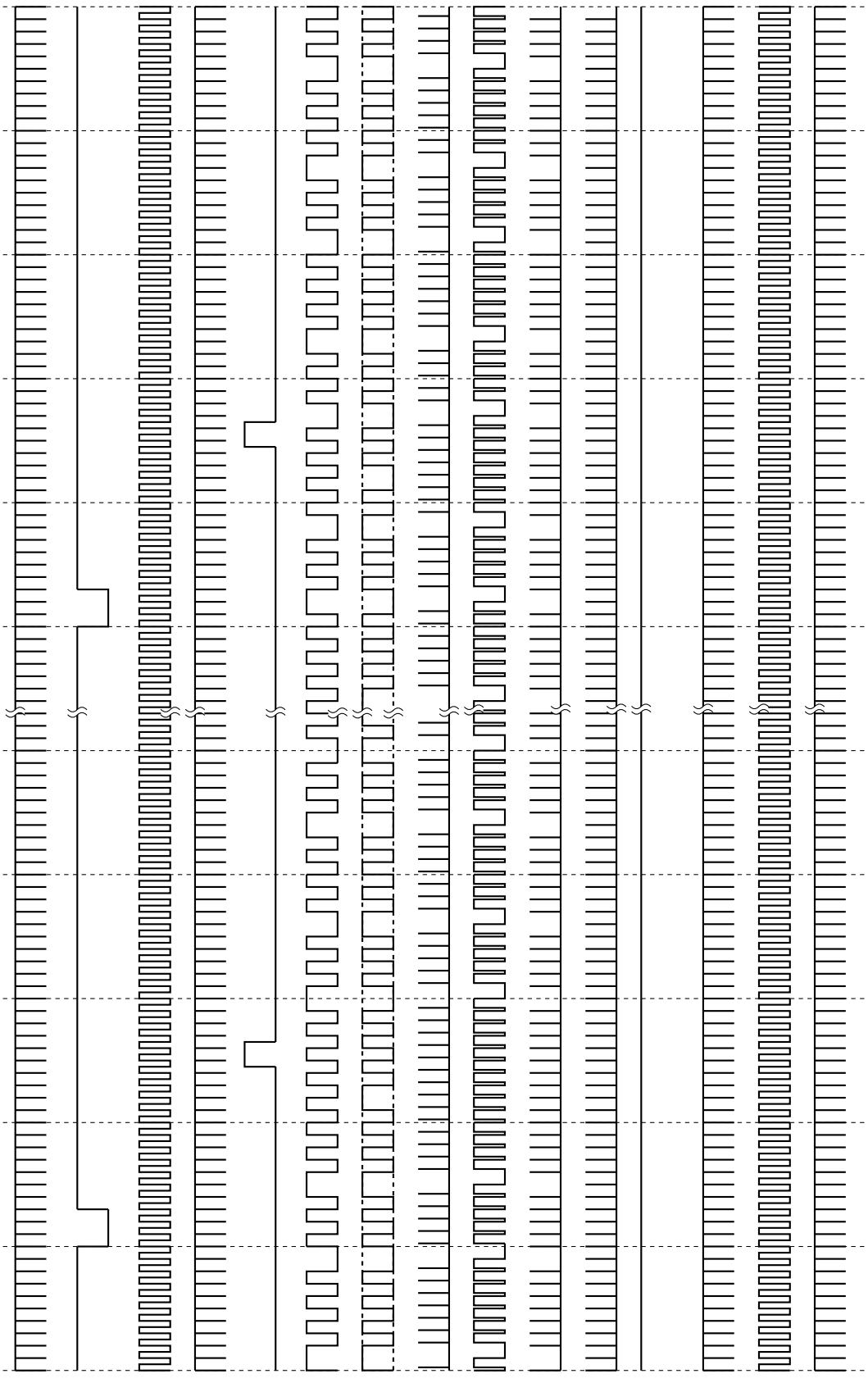
Data register setting: VB1 = 0 or VB2 = 0, VP = 01E/h, other settings = default
(Example for input signal with total number of vertical lines = 1000)



* The 1H and 1V cycle FRP polarity is not specified.

Vertical Direction Timing Chart

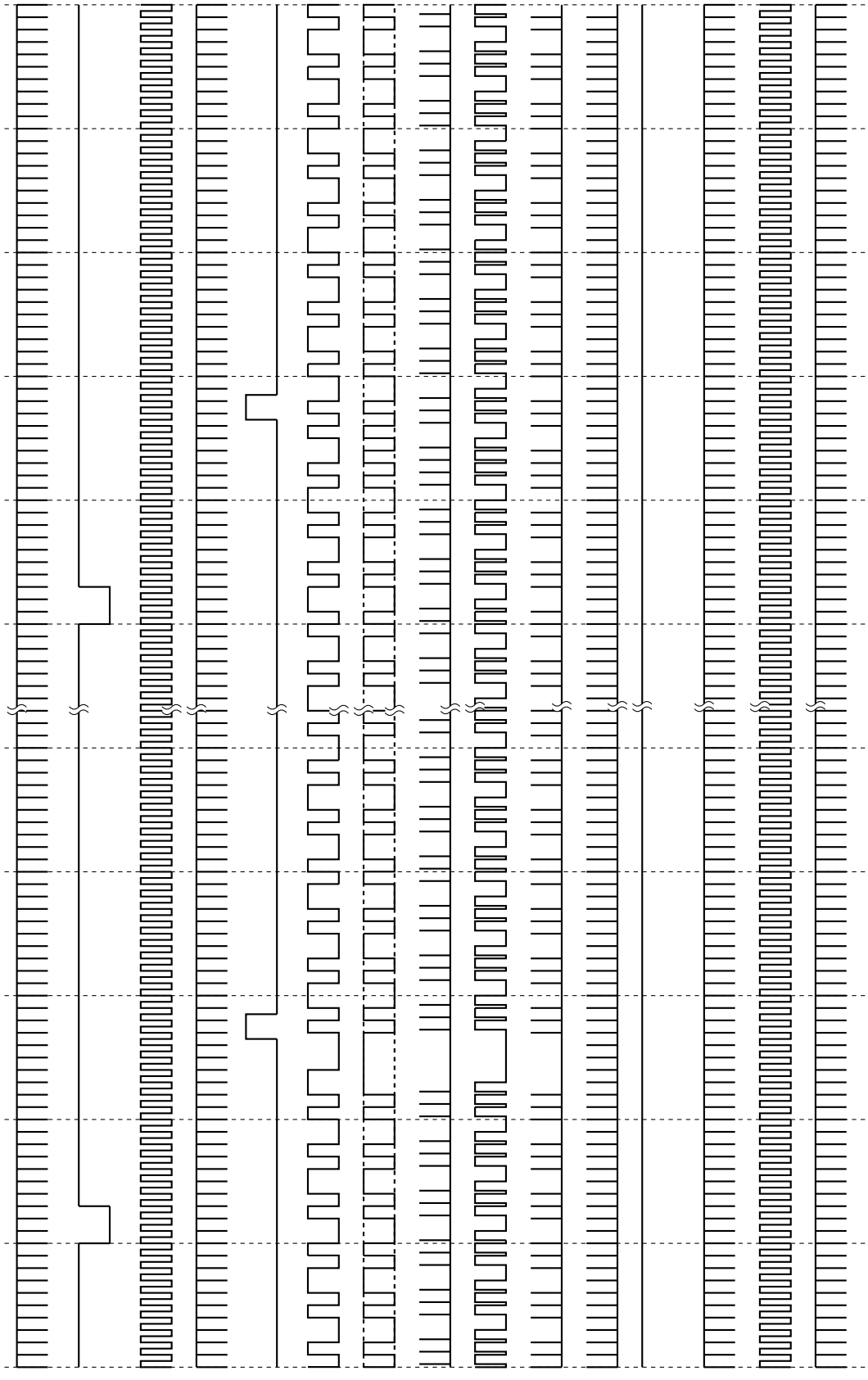
Data register setting: MBK0 = 1, MBK1 = 0, VP = 00A/h, other settings = default
(Example for input signal with total number of vertical lines = 1250)



* The 1H and 1V cycle FRP polarity is not specified.

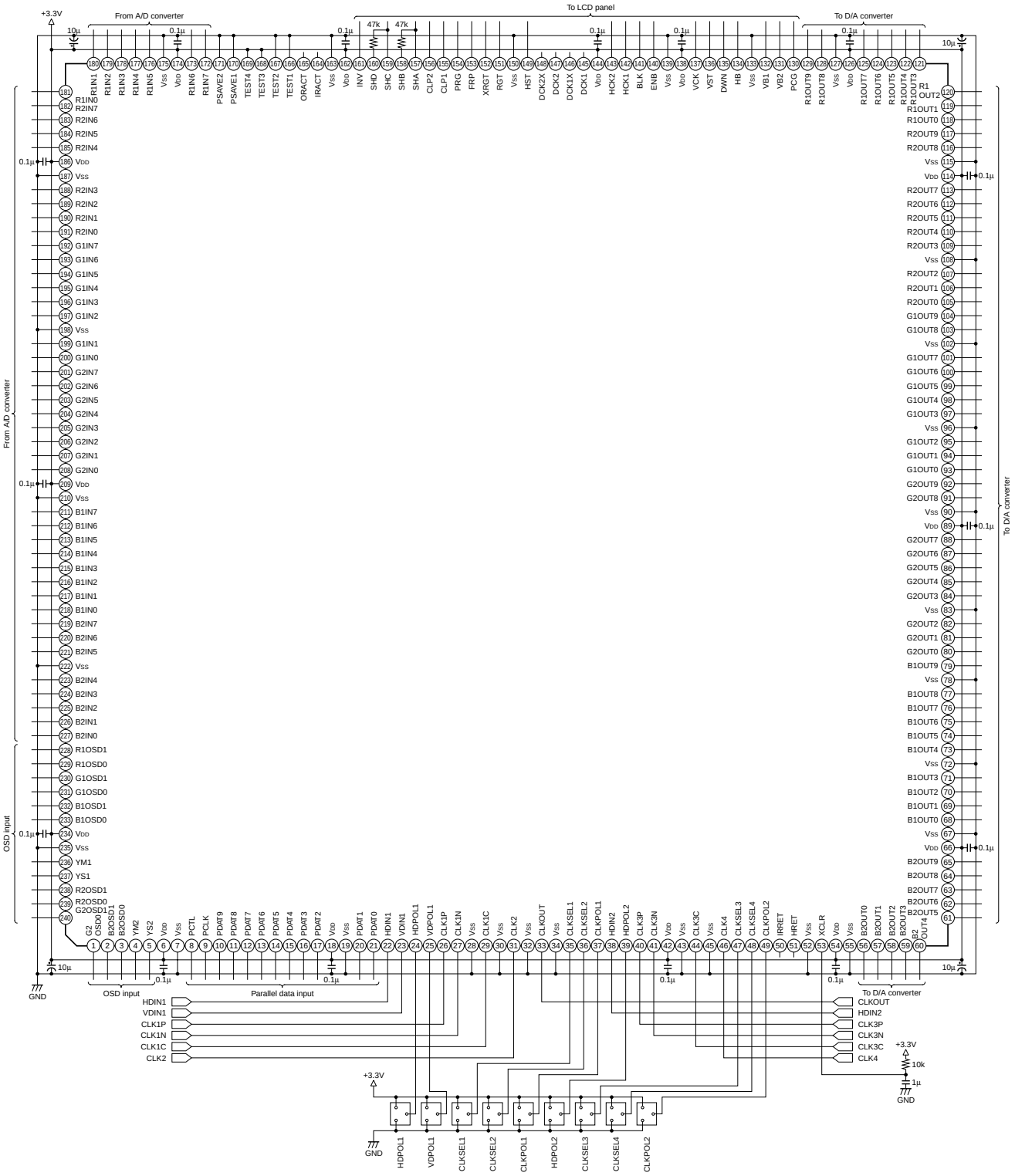
Vertical Direction Timing Chart

Data register setting: MBK0 = 1, MBK1 = 1, VP = 00C/h, other settings = default
(Example for input signal with total number of vertical lines = 1066)



* The 1H and 1V cycle FRP polarity is not specified.

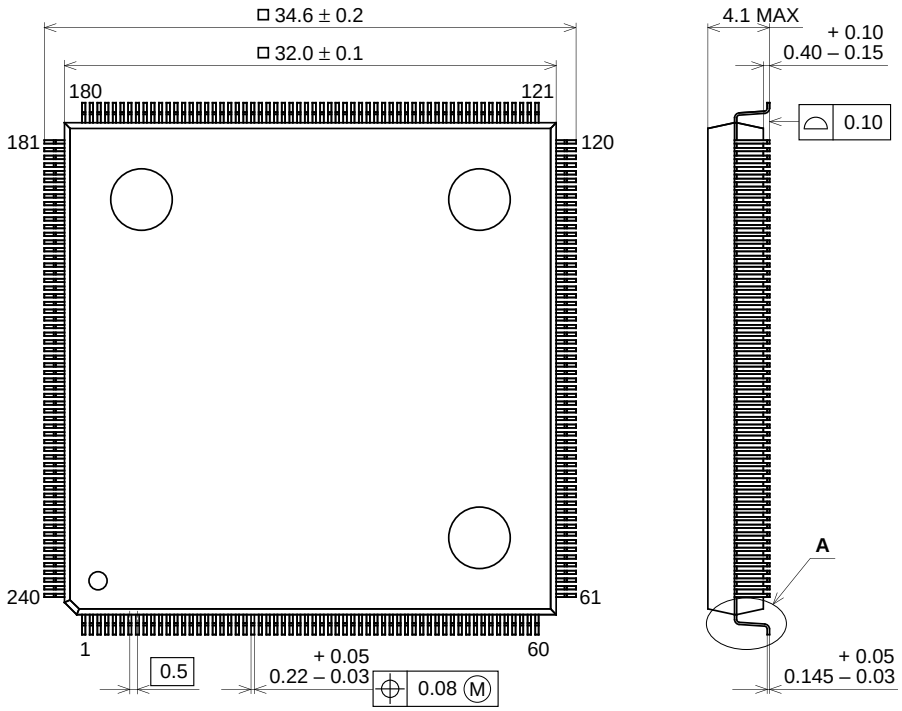
Application Circuit

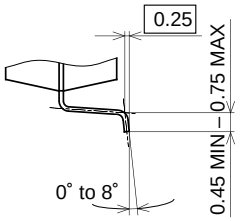


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

240PIN QFP (PLASTIC)





DETAIL **A**

SONY CODE	QFP-240P-L022
EIAJ CODE	QFP240-P-3232
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	7.6g